Tektronix®

8540
INTEGRATION UNIT
INSTALLATION GUIDE
SERVICE

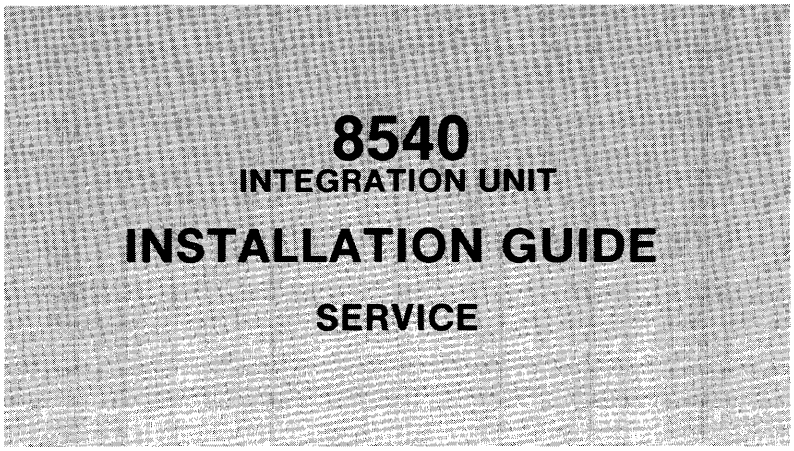
INSTRUCTION MANUAL

Tektronix®
COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.



Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

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PREFACE

INTRODUCTION

This manual contains information on how to install an 8540 Integration Unit. Since this is an Installation Guide, and not a User's Manual, this book contains few operating instructions other than those required to perform system verification.

The 8540 Integration Unit should be installed by a Tektronix Field Service Specialist. Tektronix, Inc. is not obligated to furnish service to repair damage resulting from attempts by unauthorized personnel to install this product. Please call your nearest Tektronix Field Service Office for installation.

ABOUT THIS MANUAL

This manual supports installation and verification of the 8540 Integration Unit. Specifically, the sections in this manual provide the following information:

Section 1 An overview to the 8540 Integration Unit.

Section 2 Specifications for the 8540 Integration Unit.

Section 3 Instructions on unpacking the 8540 and setting up a work site.

Section 4 8540 front and rear panel controls, connectors, and indicators.

Section 5 Verification that the 8540 Integration Unit is working properly.

Section 6 How the 8540 is configured when operating with other equipment.

Section 7 8540 Integration Unit circuit board configurations.

NOMENCLATURE

Throughout this manual, the following terms are used for the sake of brevity.

Term	Meaning
8540	8540 Integration Unit
8560	8560 Multiuser Software Development Unit
System Terminal	The terminal used for command entry and connected to the 8540

CHANGE INFORMATION

Change notices are issued by Tektronix, Inc., to document changes in the manual after it has been published. Change information is located in the back of this manual, following the yellow tab marked "CHANGE INFORMATION & TEST EQUIPMENT". When you receive this manual, enter any change information into the body of the manual, as indicated on the change notice.

REVISION HISTORY

As this book is revised and reprinted, revision history information is included in the text and diagrams. Original manual pages are indicated by the "@" symbol at the bottom inside corner of the page. Existing pages of manuals that have been revised are indicated by a revision code and date (REV B SEP 1981) in place of the "@" symbol. New pages added to an existing section, whether they contain old, new, or revised information, contain the "@" symbol alongside the revision date (@ SEP 1981).

MANUAL OVERVIEW

The 8540 Integration Unit is supported by a variety of user and servicing manuals. 8540 user manuals contain operating instructions for the 8540, and are standard accessories. 8540 servicing manuals consist of installation and service manuals. The installation manual contains instructions for 8450 installation and system verification. This manual is a standard accessory. The 8540 service manual contains servicing information for the basic 8540 configuration. Service manuals are optional accessories that must be ordered separately.

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Section 2 --SPECIFICATIONS

Section 3 -- UNPACKING THE 8540

Section 4 — 8540 CONTROLS, CONNECTORS, AND INDICATORS

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

As Marked on Equipment


DANGER high voltage.


Protective ground (earth) terminal.


ATTENTION - Refer to manual.

SAFETY PRECAUTIONS

GROUNDING THE 8540

The 8540 Integration Unit is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the equipment's power input terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your 8540.

Use only a power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

USE THE PROPER FUSE

To avoid fire hazard, use only the fuse specified in the parts list for your 8540. Be sure the fuse is identical in type, voltage rating, and current rating.

Refer fuse replacement to qualified service personnel.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate the 8540 in an atmosphere of explosive gases.

DO NOT REMOVE COVERS OR PANELS

To avoid personal injury, do not remove covers or panels from the 8540. Do not operate the 8540 without the covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

(Refer also to the preceding Operators Safety Summary)

DO NOT SERVICE ALONE

Do not perform internal service or adjustment on the 8540 unless another person capable of rendering first aid and resuscitation is present.

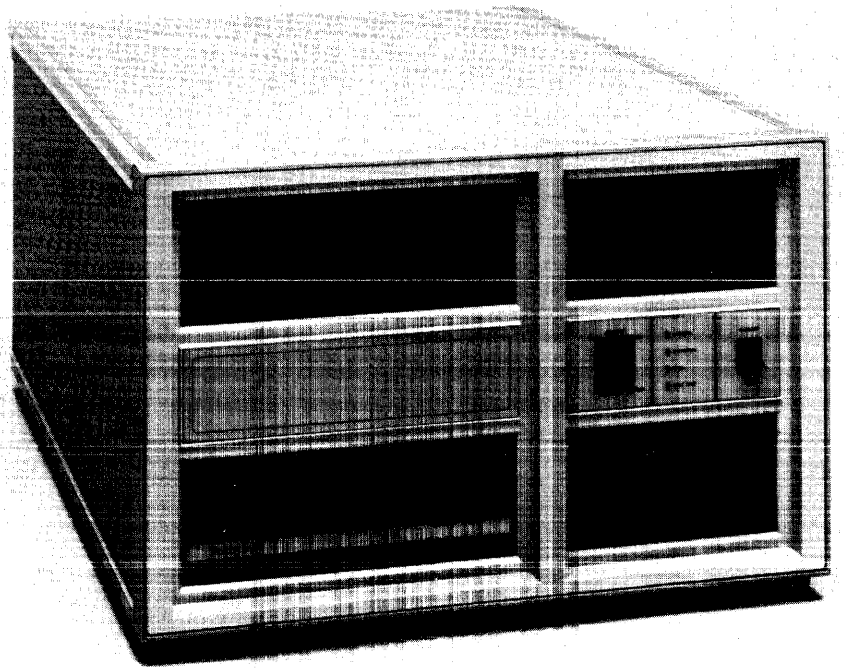
USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in the 8540. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

POWER SOURCE

The 8540 is designed to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.



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8540 Integration Unit

Section 1

8540 OVERVIEW

INTRODUCTION

This section briefly describes the 8540 Integration Unit (IU) and the host computer support associated with the 8540. This section also examines the 8540 on a functional block level to provide an idea of how the system operates.

WHAT IS AN 8540?

The 8540 is a distributed, hardware/software integration work station. In conjunction with a host computer and software development tools, it forms a complete Microcomputer Development System. This system provides the tools for testing microcomputer programs and prototype designs, including in-circuit-emulation and PROM programming. The external computer (host) is used for all software development, mass storage, and file management. The files are prepared on the host computer where they are edited, compiled, linked, and then downloaded to the 8540. Emulation may then be performed by using unique emulator processors in the 8540. The emulator processors are optional equipment to the 8540 and configured for specific microprocessors/microcomputers.

The 8540/Host development system is controlled through a system terminal, which is usually attached to the 8540. In some instances, the terminal may be attached to the host computer.

The software for the 8540 (operating system) and associated optional equipment is contained in ROMs. In addition, the 8540 has 4K bytes of non-volatile EEPROM. This is partitioned into two areas; one area stores 8540 command strings and the other area stores revisions and update information. Command strings and revisions can be made in the field via the system terminal. Command strings are stored using the PERMSTR command and recalled using the string name. Revisions or updates to the operating system are entered using the ROMPATCH command. The operating system implements the revisions (patches) after loading the ROM contents into RAM, and before executing the affected software.

The 8540 has built-in diagnostics that are executed at power-up to verify proper operation of the basic system. In addition, ROM-based diagnostics provide fault isolation for the standard 8540 configuration. Fault isolation is also provided as a standard accessory to each optional board.

8540 CONFIGURATION

The 8540 is primarily an emulating machine with software/hardware debugging capabilities. The 8540 contains the following standard circuit boards:

System Controller	The main controlling element for the 8540.
Communications Interface	This board performs the TTL-to-RS-232 and high-speed serial interface (HSI) signal conversion.
System RAM	This 64K dynamic RAM is used to store the 8540 operating system.
System ROM	Contains the 8540 operating system software in ROMs.
Emulator Controller	The 8540 bus arbiter.
Program Memory	This 32K-byte static RAM is used to store programs downloaded from the host computer.
Front Panel	This board contains the Front Panel controls and LEDs.

Figure 1-1 is a simplified block diagram of the 8540.

In addition to the standard circuit boards, the 8540 has plug-in capability for the following optional equipment:

- Program Memory --- Additional Program Memory boards are available to expand the program memory from 32K to 128K bytes.
- Emulator Processors --- Two 8-bit emulator processors (consisting of one circuit board each) or one 16-bit emulator may be installed at any one time.
- Trigger Trace Analyzer (TTA) --- This option consists of two boards: Trigger Trace #1 and Trigger Trace #2.
- PROM Programmer circuit board.
- MAC (Memory Allocation Controller) --- Provides memory relocation for 16-bit emulators.

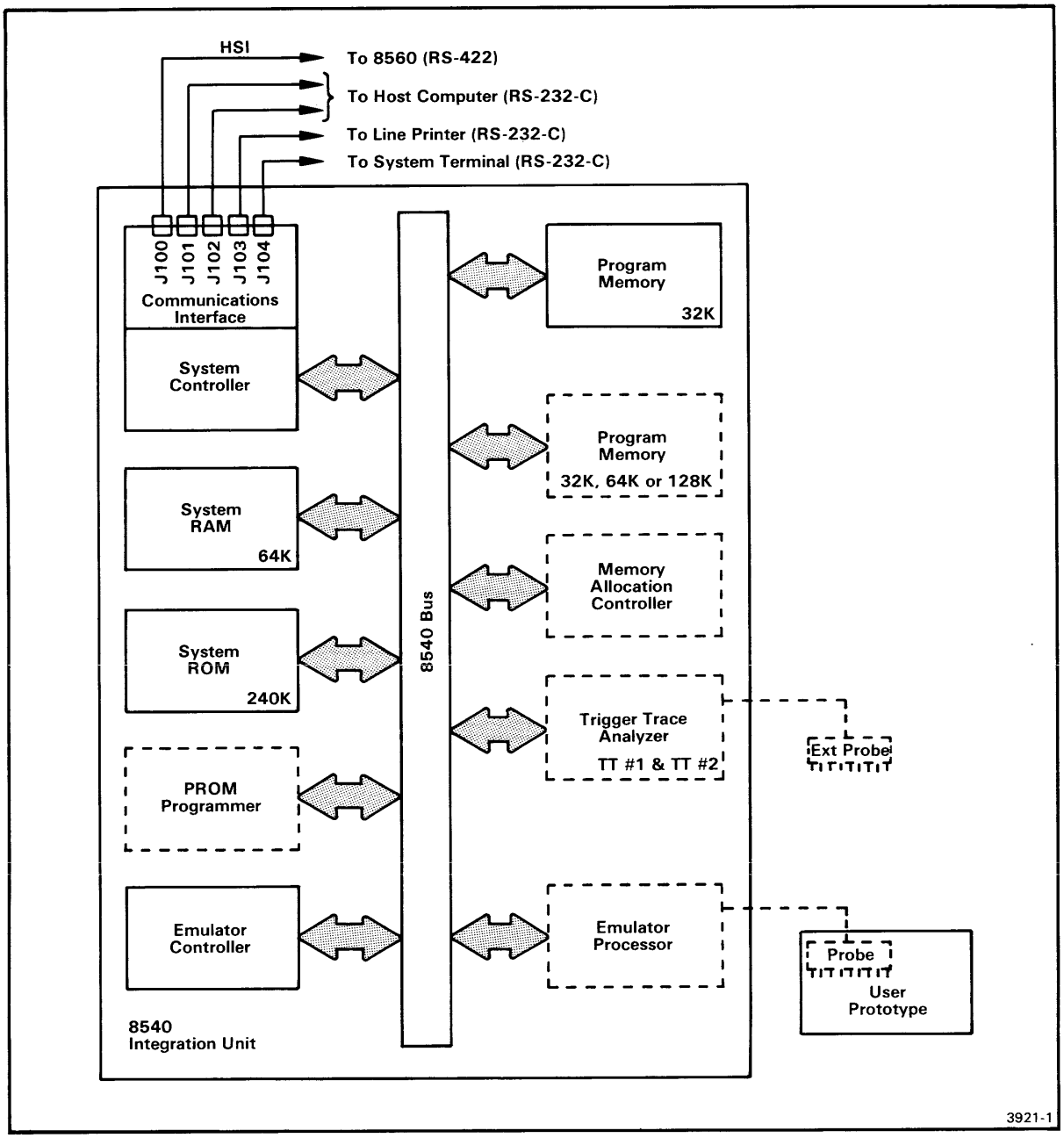

Fig. 1-1. 8540 Integration Unit block diagram.

SYSTEM CONTROLLER

The System Controller board contains the system processor (2650A-1) which is the main controlling element for the 8540. The system processor serves as the "master" in the master/slave environment of the 8540. The System Controller board handles communications for the 8540, as well as debugging and system utility program execution.

COMMUNICATIONS INTERFACE

The Communications Interface board is attached to the rear panel of the 8540, and converts the TTL signals from the System Controller into RS-232 or RS-422 compatible signals.

SYSTEM RAM

The System RAM board is a 64K dynamic RAM. The System RAM is used to store the 8540 operating system (OS/40), which is contained in ROMs on the System ROM board. The System RAM board is restricted to operating on the system side of the Emulator Controller in the Main Interconnect board.

SYSTEM ROM

The System ROM board consists of two memory arrays: 240K ROM and 4K EEPROM arrays. The 8540 operating system and optional equipment software are contained in the 240K ROM array. The revisions/updates (patches) to the software programs in the 240K ROM array are made in the 4K EEPROM array. A PROM programmer accesses the EEPROMs under control of the 8540 operating system in response to commands from the terminal.

EMULATOR CONTROLLER

The Emulator Controller board is the bus arbiter for the 8540. The 8540 is basically a multi-processor machine, and the Emulator Controller makes sure that only one processor has control of the buses at a time. The Emulator Controller also contains breakpoint, forced jump, and program counter circuitry used during debugging operations.

PROGRAM MEMORY

The Program Memory is a 32K-byte static RAM. This memory is used to store the programs that are downloaded from the host computer. A second Program Memory board (optional) may be added to increase the Program Memory to 64K. Additional memory boards (optional) may be added to increase the amount of program memory to 128K bytes.

ACCESSORIES

STANDARD ACCESSORIES

The following standard accessories are included with the 8540:

- Power cord
- 8540 Integration Unit System Users Manual
- 8540 Integration Unit Installation Guide

OPTIONAL ACCESSORIES

Optional accessories for the 8540 may be obtained through your nearest Tektronix Field Service Office. The following optional accessories are available at this printing:

- 8540 Integration Unit Service Manual -- 070-3920-XX
- Extender Board -- 067-0828-01
- Wrap-back connectors -- 067-1020-00
  (male and female connectors used for diagnostic testing of the peripheral ports)
- HSI Communication Cables (for interface connection to Tektronix 8560 Multi-User Software Development System), in the following lengths:
  8 feet (2.4 m) -- 012-1009-00
  20 feet (6.1 m) -- 012-1008-00
  50 feet (15.2 m) -- 012-1007-00
  250 feet (76.2 m) -- 012-1010-00
- RS-232-C interface cable for general modem or direct host computer connection:
  15 feet (4.6 m) -- 012-0757-00

Section 2

SPECIFICATIONS

INTRODUCTION

This section contains the specifications for the 8540. Tables 2-1, 2-2, and 2-3 list the specifications for the 8540 as a whole. Table 2-4 lists the power requirements for each circuit board within the basic 8540 unit. Table 2-5 lists the specifications for EEPROM voltage Vpp during read and write operations. Tables 2-6 through 2-13 contain the 8540 I/O port characteristics for all connectors on the 8540 rear panel. These tables define the peripheral interface requirements.

Table 2-1
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
Primary Power Input Voltages	115 Vac Low (a)	90--110 Vac
	115 Vac High (a)	108--132 Vac
	230 Vac Low (a)	180--220 Vac
	230 Vac High (a)	216--250 Vac
Frequency		49--63 Hz
Line Fuses 115 Vac		3AG, 8 Amps, 250 Volt, medium-blow (5 sec.)
230 Vac		3AG, 4 Amps, 250 Volt, medium-blow (5 sec.)
Line Current (maximum)		7 Amps
Power Consumption (maximum)		700 Watts

Table 2-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Power Supply	+5.2 Vdc +1%/-2% (b)	With all boards installed in unit. Do not exceed maximum current of 35 Amps.
	+12.0 Vdc +/- 5% (b)	With all boards installed in unit. Do not exceed maximum current of 1.7 Amps.
	-12.0 Vdc +/- 5% (b)	With all boards installed in unit. Do not exceed maximum current of 1.7 Amps.
Heat Dissipation Typical		684 BTU/hr
Maximum		1,227 BTU/hr
Static Discharge Operating Front Panel LEDs		12.5 kV and below with no effect on operation of unit
Except for Front Panel LEDs		15 kV and below with no effect on operation of unit NOTE Static voltage must not be applied to the pins of any external connector.
Line Regulation		Within .05% for 10% line voltage change
Load Regulation		Within .05% for 50% load change

(a) Set switches S300 and S301 to one of the listed operating positions, determined by the primary voltage source. See Section 4, 8540 Controls, Connectors, and Indicators, for additional information on setting these switches.

(b) Refer to the 8540 Service Manual if these voltages are out of tolerance.

Table 2-2
Environmental Characteristics

Characteristic	Description
Temperature	
Operating	0 C to +50 C (+32 F to +122 F)
Storage	-55 C to +75 C (-67 F to +167 F)
Humidity	
Operating	To 90% relative non-condensing
Altitude	
Operating	To 4 500 m (15,000 feet)
Storage	To 15 000 m (50,000 feet)

Table 2-3
Physical Characteristics

Characteristic	Description
Net Weight	27 kg (60 lb.)
Overall Dimensions	
Height	267 mm (10.5 in.)
Width	432 mm (17 in.)
Length	597 mm (23.5 in.)

Table 2-4
Circuit Board Power Requirements

Circuit Board	Voltage	Typical Amps	Maximum Amps
System Controller	+12 Vdc	0.019	0.023
	-12 Vdc	0.018	0.022
	+5 Vdc	2.7	3.24
Communications Interface	+12 Vdc	0.019	0.023
	-12 Vdc	0.018	0.022
	+5 Vdc	0.20	0.24
Emulator Controller	+5 Vdc	1.4	1.68
Front Panel	+5 Vdc	0.072	0.113
System RAM	+5 Vdc	1.555	2.117
System ROM	+5 Vdc	2.05	2.46
Not Programming	+12 Vdc	0.0125	0.015
Programming	+12 Vdc	0.050	0.060
Program Memory	+5 Vdc	3.8	4.56

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Table 2-5
System ROM Board -- EEPROM Voltage Vpp
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
Voltage at TP Vpp		
During Read Operations	+5.0 Vdc +/- 1 Volt	The voltage at this test point is the Vpp voltage applied to the EEPROMs during a read operation.
During Write Operations (when progamming EEPROMs)	+21.0 Vdc +/- 1 Volt	The voltage at this test point is the Vpp voltage applied to the EEPROMs during a write operation (erase or programming).
Time Constant		
Voltage at TP Vpp 600 us after start of pulse, when starting a write operation. (during EEPROM programming)	+15.0 Vdc +/- 1 Volt	Refer to Fig. 2-1.

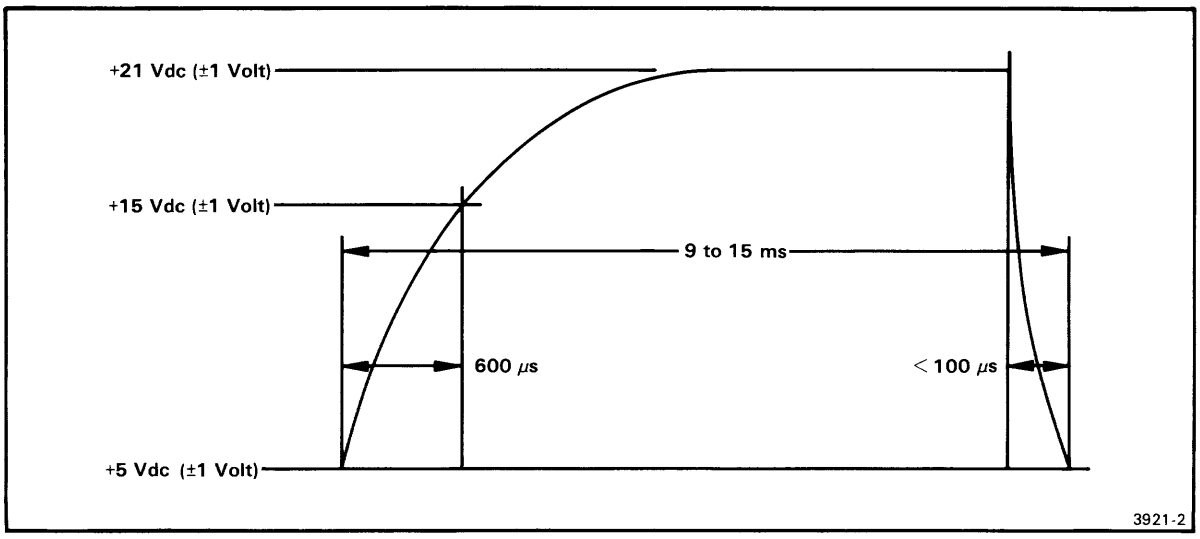


Fig. 2-1. Time constant for Vpp during programming.

Table 2-6
8540 I/O Port Characteristics
HSI Port Specifications -- J100

Characteristics	Description
Type	RS-422
Baud Rate	HSI -- 153.6K Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Even
Signal Descriptions:	
Pin 1	Shield
Pin 2	TX -- Transmit Data
Pin 3	RX -- Receive Data
Pin 4	RTS -- Request To Send (pulled-up to +5 Vdc with 200 ohm resistor)
Pin 5	CTS -- Clear To Send
Pin 10	RTS' -- Request To Send (always grounded)
Pin 11	TX' -- Transmit Data
Pin 12	RX' -- Receive Data
Pin 13	DTR' -- Data Terminal Ready
Pin 20	DTR -- Data Terminal Ready
Pin 25	CTS' -- Clear To Send

Table 2-7
8540 I/O Port Characteristics
Remote Port Specifications With DTE1 Selected -- J101
(Configured as a DTE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110--9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to TxD output on ACIA Type 6850 - U2600-6)
Pin 3	RX -- Receive Data (connected to RxD input on ACIA Type 6850 - U2600-2)
Pin 4	RTS -- Request To Send (connected to RTS output on ACIA Type 6850 - U2600-5)
Pin 5	CTS -- Clear To Send (connected to CTS input on ACIA Type 6850 - U2600-24)
Pin 6	DSR -- Data Set Ready (ignored - connected to input of receiver Type 1489 - U3060D)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (connected to DCD input on ACIA Type 6850 - U2600-23)
Pin 20	DTR -- Data Terminal Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)

NOTE

The 8540 looks at CTS to implement the handshake on data transmissions from the peripheral to the 8540.

Table 2-8
8540 I/O Port Characteristics
Remote Port Specifications With DTE2 Selected -- J101
(Configured as a DTE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110--9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to TxD output on ACIA Type 6850 - U2600-6)
Pin 3	RX -- Receive Data (connected to RxD input on ACIA Type 6850 - U2600-2)
Pin 4	RTS -- Request To Send (connected to RTS output on ACIA Type 6850 - U2600-5)
Pin 5	CTS -- Clear To Send (ignored - connected to input of receiver Type 1489 - U3060C)
Pin 6	DSR -- Data Set Ready (connected to CTS input on ACIA Type 6850 - U2600-24)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (connected to DCD input on ACIA Type 6850 - U2600-23)
Pin 20	DTR -- Data Terminal Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)

NOTE

The 8540 looks at DSR to implement the handshake on data transmissions from the peripheral to the 8540.

Table 2-9
8540 I/O Port Characteristics
Remote Port Specifications With CNTL(L) Selected -- J101
(Configured as a DTE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110--9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to TxD output on ACIA Type 6850 - U2600-6)
Pin 3	RX -- Receive Data (connected to RxD input on ACIA Type 6850 - U2600-2)
Pin 4	RTS -- Request To Send (Jumper J2 on Communications Interface board selects CTS as the RTS output or continuously asserts RTS. RTS is continuously asserted for normal operation.)
Pin 5	CTS -- Clear To Send (ignored - connected to input of receiver Type 1489 - U3060C)
Pin 6	DSR -- Data Set Ready (ignored - connected to input of receiver Type 1489 - U3060D)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (ignored - connected to input of receiver Type 1489 - U3060A)
Pin 20	DTR -- Data Terminal Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)

NOTE

This configuration requires only TX, RX, and ground to be implemented by the peripheral in order to transfer data. No handshaking can take place in this configuration.

Table 2-10
8540 I/O Port Characteristics
Remote Port Specifications With CNTL(L) Selected -- J102
(Configured as a DCE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110--9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to RxD input on ACIA Type 6850 - U2600-2)
Pin 3	RX -- Receive Data (connected to TxD output on ACIA Type 6850 - U2600-6)
Pin 4	RTS -- Request To Send (ignored - connected to input of receiver Type 1489 - U3060A)
Pin 5	CTS -- Clear To Send (Jumper J1 on Communications Interface board selects RTS as the CTS output or continuously asserts CTS. CTS is continuously asserted for normal operation.)
Pin 6	DSR -- Data Set Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 20	DTR -- Data Terminal Ready (ignored - connected to input of receiver Type 1489 - U3060D)

NOTE

This configuration requires only TX, RX, and ground to be implemented by the peripheral in order to transfer data. No handshaking can take place in this configuration.

Table 2-11
8540 I/O Port Characteristics
Remote Port Specifications With DCE Selected -- J102
(Configured as a DCE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110--9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to RxD input on ACIA Type 6850 - U2600-2)
Pin 3	RX -- Receive Data (connected to TxD output on ACIA Type 6850 - U2600-6)
Pin 4	RTS -- Request To Send (connected to DCD input on ACIA Type 6850 - U2600-23)
Pin 5	CTS -- Clear To Send (connected to RTS output on ACIA Type 6850 - U2600-5)
Pin 6	DSR -- Data Set Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 20	DTR -- Data Terminal Ready (connected to CTS input on ACIA Type 6850 - U2600-24)

NOTE

DTR must be used to control data transmission from the 8540 to the peripheral. RTS/CTS are used to control data transmission from the peripheral to the 8540.

Table 2-12
8540 I/O Port Characteristics
Auxiliary Port Specifications -- J103
(Configured as a DCE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110--9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to RxD input on ACIA Type 6850 - U2500-2)
Pin 3	RX -- Receive Data (connected to TxD output on ACIA Type 6850 - U2500-6)
Pin 4	RTS -- Request To Send (connected to DCD input on ACIA Type 6850 - U2500-23)
Pin 5	CTS -- Clear To Send (connected to RTS output on ACIA Type 6850 - U2500-5)
Pin 6	DSR -- Data Set Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 17	External Clock
Pin 20	DTR -- Data Terminal Ready (connected to CTS input on ACIA Type 6850 - U2500-24)

NOTE

DTR must be used to control data transmission from the 8540 to the peripheral. RTS/CTS are used to control data transmission from the peripheral to the 8540.

Table 2-13
8540 I/O Port Characteristics
Terminal Port Specifications -- J104
(Configured as a DCE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110--9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to RxD input on ACIA Type 6850 - U2700-2)
Pin 3	RX -- Receive Data (connected to TxD output on ACIA Type 6850 - U2700-6)
Pin 4	RTS -- Request To Send (connected to DCD input on ACIA Type 6850 - U2700-23)
Pin 5	CTS -- Clear To Send (connected to RTS output on ACIA Type 6850 - U2700-5)
Pin 6	DSR -- Data Set Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 20	DTR -- Data Terminal Ready (connected to CTS input on ACIA Type 6850 - U2700-24)

NOTE

DTR must be used to control data transmission from the 8540 to the peripheral. RTS/CTS are used to control data transmission from the peripheral to the 8540.

Section 3

UNPACKING THE 8540

INTRODUCTION

In this section, we'll discuss the steps involved in unpacking and installing the 8540. The following subjects are included:

- o site preparation, including space and power requirements;
- o unpacking the 8540, including storage and reshipping; and
- o preparing the 8540 for operation.

SITE PREPARATION

The first consideration in selecting a work site is space. Two other criteria for selecting a work station are power requirements and environmental conditions. We'll discuss each of these points in turn.

SPACE REQUIREMENTS

The 8540 dimensions are shown in Fig. 3-1.

Here are some things to consider when setting up a work station for the 8540:

- o Provide adequate ventilation for the 8540.
- o Allow enough room at the rear of the unit for proper cable dress.
- o Storage space should be close at hand for manuals and other documents.
- o Space may be required for ongoing hardware development projects.
- o Space will be required for a system terminal and perhaps a line printer.
- o You will need to gain access to the inside of the unit, so make sure adequate space is available behind and to the sides of the unit for removing the top cover (the unit should be rotated 180 degrees when removing the top cover).

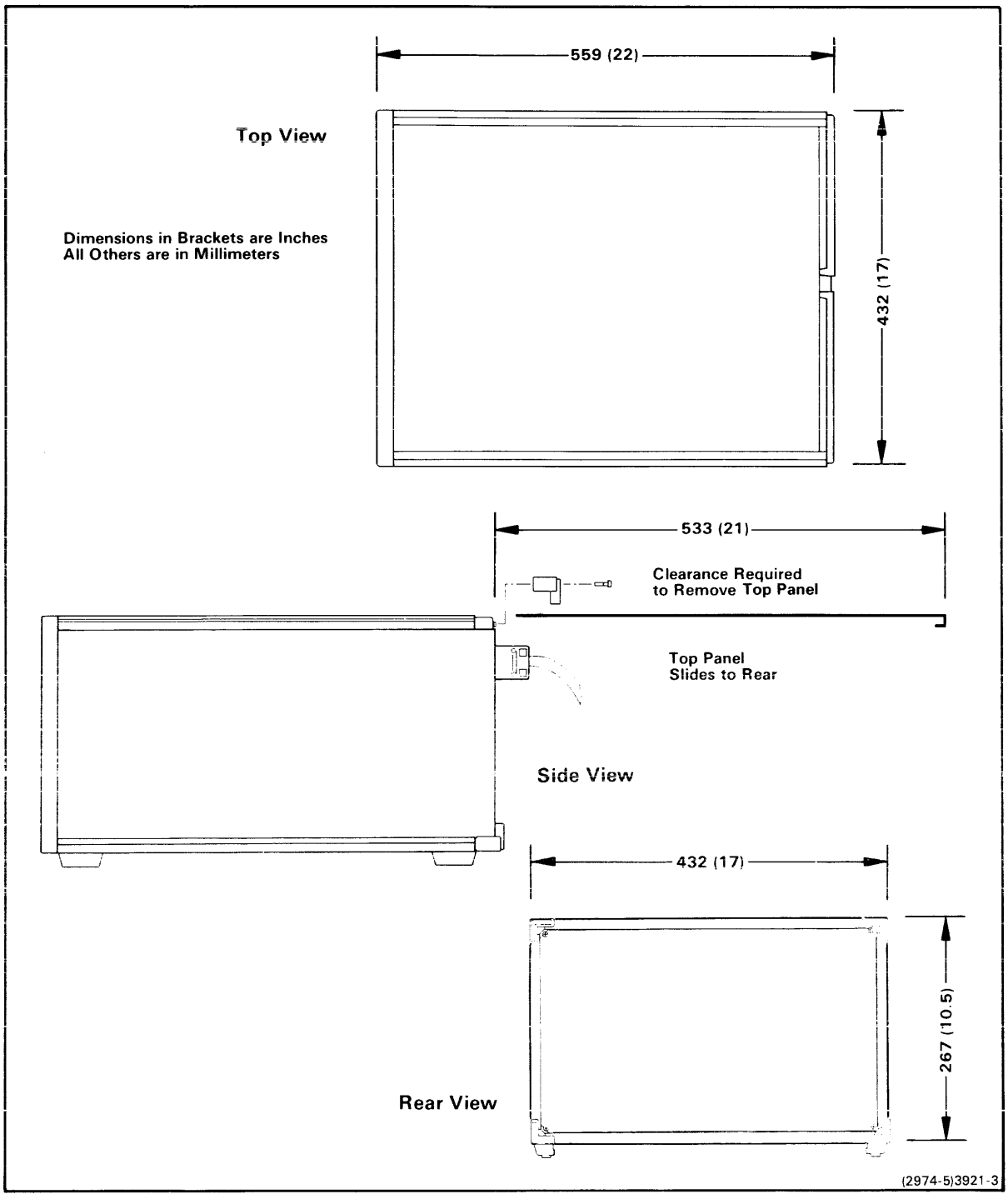


Fig. 3-1. Dimensions of the 8540.

POWER REQUIREMENTS

The primary power requirements for the 8540 are as follows:

Line Voltages	115 Vac Low (90--110 Vac) 115 Vac High (108--132 Vac) 230 Vac Low (180--220 Vac) 230 Vac High (216--250 Vac)
Line Frequency	49--63 Hz
Line Current (maximum)	7 Amps
Power Consumption (maximum)	700 Watts

When preparing a work site for the 8540, observe the following:

1. All peripheral components at the work area must share common ground and neutral lines to avoid noisy grounds and ground loops.
2. All units must be properly grounded.
3. The work area should be on a separate power breaker switch.

ENVIRONMENTAL CONSIDERATIONS

The following considerations should be taken into account when preparing the work site.

- The area selected for the work station should be adequately lighted, air-conditioned, and dust-free.

CAUTION

Static electricity may damage components of the 8540. Use standard anti-static procedures when setting up the work site.

- The work area should be as static-free as possible. If carpeting is used, the carpet must be static-free and treated with anti-static chemicals as often as required.
- The 8540 should be placed on a static-free work surface.
- Allowances must be made for adequate air exhaust at the rear of the unit (6" minimum).

UNPACKING THE 8540

Before you unpack the 8540, examine the carton for external damage. If you find any damage:

- Immediately notify the carrier who made delivery, and request inspection.
- Contact your nearest Tektronix Field Engineering Office or sales representative.
- Do not throw away the boxes.
- DO NOT TRY TO REPAIR THE INSTRUMENT.

REMOVING THE 8540 FROM THE CARTON

The 8540 unit is packed in a heavy-duty cardboard container, surrounded by foam packing material. A piece of cardboard covers the top of the unit. The power cord and options rest on the cardboard.

When you open the carton, remove the power cord and any other material that may rest on the cardboard, and set them aside. Remove the cardboard and set it aside.

WARNING

Use caution when lifting the 8540 out of the box. The 8540 weighs 27 kg (60 pounds). Don't hurt yourself -- get some help.

Remove the 8540 and surrounding foam. Set the packing material aside. (Don't lose the packing material -- you'll need it again if you ever have to ship the 8540.)

STORAGE AND RESHIPPING

When a precision electronic instrument, such as the 8540, is to be stored or reshipped, it's best to repack it as it was originally shipped from the factory. For this reason, be sure to save the carton and packing material in which your equipment was shipped. To repack the 8540, simply follow the unpacking instructions in reverse order. The following paragraphs describe further considerations that must be made when storing or reshipping an 8540.

Storage

Observe the following considerations whenever you place the 8540 in storage:

- Provide adequate protection from dust.
- Do not exceed the humidity or temperature limitations of the instrument, as outlined in Section 2, Specifications of this manual.
- Store the carton upright. Do not compress the carton or stack heavy objects upon it.

Reshipping

If the unit must be shipped to the factory or service center, the following steps should be taken:

1. Note the serial number of the unit on the back panel and any other relevant numbers or symbols needed for identification. (This information is required for fault notification correspondence, which should be sent separately.)
2. Wrap the unit in durable waterproof material such as heavy polyethylene, and tape securely. This step should be carried out only in a dry atmosphere, and with the unit cool to the touch.
3. Pack the unit in a sturdy box (heavy cardboard is acceptable for land shipments), lined with 76 mm (3 in.) of medium-density foam or expanded polystyrene.
4. Cables, adapters, and other accessories should be wrapped separately and attached by tape to the inner liner at a break in the foam, or taped to a separate platform mounted above the foam or polystyrene (as used in the original shipping). In the latter case, a sheet of 25 mm (1 in.) minimum thickness foam should be taped above the cable package.
5. Seal the carton with reinforced packaging tape. Identify the sender, the unit number, and the serial number on the outside of the carton.
6. Before you ship an 8540, notify the factory or your sales representative of your intent to ship the instrument, and await their acknowledgement.

PREPARING THE 8540 FOR OPERATION

After removing the 8540 from its packing carton, set it on a flat surface, preferably the work site. Examine the outside of the 8540 for any damage that may have occurred during shipping. If damage is found, follow the procedure given before.

Set the 8540 on the surface so that you are facing the rear panel. Using a Phillips screwdriver, remove the two upper cover retainers, as shown in Fig. 3-2. Slide the top cover back and off the 8540.

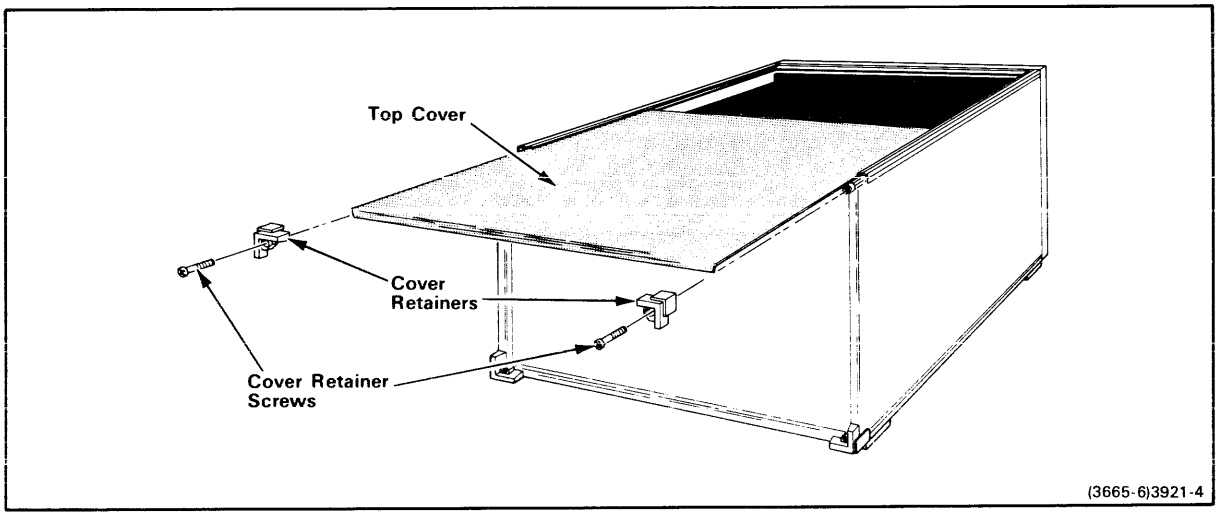


Fig. 3-2. Removing the 8540 top cover.

Notice inside the 8540 that a cardboard and foam restrainer covers the circuit boards. The restrainer holds the circuit boards in place during transit. Lift the restrainer from the unit. Store the restrainer with the packing materials in case you need it later.

Examine the inside of the 8540 for any loose circuit boards, cables, or connectors. If you see any damage, follow the procedure given for reporting damage.

Replace the top cover and the two cover retainers, according to the following procedure. Information on the installation of options is given in the installation manual for the specific option.

REPLACING THE TOP COVER

To replace the top cover of the 8540, perform the following steps:

1. From the rear panel, slide the top cover into the two grooves along the top edges of the mainframe. See Fig. 3-2.

2. Continue to insert the top cover into the grooves, until the right-angle flange at its rear edge is flush with the rear panel of the 8540.

3. Place a cover retainer at each upper rear corner of the 8540, covering the right-angle flange of the top cover.

4. Thread the two screws (removed with the top cover) through the cover retainers and tighten both screws.

REMOVING OR INSTALLING A CIRCUIT BOARD

To remove or install a circuit board in the 8540, perform the following procedure:

1. Verify that power to the 8540 is OFF.

2. Remove the 8540 top cover, according to the procedure given earlier in this section.

3. To remove a board, face the front of the 8540, grasp the ejector levers at the upper edges of the circuit board, and lift up on the levers. Pull the board straight up and free of the vertical guides. Then proceed to step 6.

4. To install a board, face the front of the 8540, grasp the ejector levers at the upper edges of the circuit board. Align the circuit board with the appropriate socket of the Main Interconnect board, so that the board's component side faces left, as you face the instrument's front panel.

5. Slide the circuit board downward, within the vertical guides, until it reaches the Main Interconnect board socket. Then, press down firmly and evenly on the upper edges of the circuit board until it snaps into place.

6. Replace the 8540 top cover, according to the procedure given earlier in this section.

RACK-MOUNT PROCEDURE

If you purchased the rack-mount option, you'll find rack-mount hardware in the bottom of the 8540 packing container. The rack-mount slides are already mounted to the sides of your 8540. You must install the slide guides in the rack frame.

Figure 3-3 illustrates the rack-mount guide orientation. Mount the guides in the rack with the hardware provided. Tighten the screws securely. Once the guides are mounted, slide the 8540 into the rack.

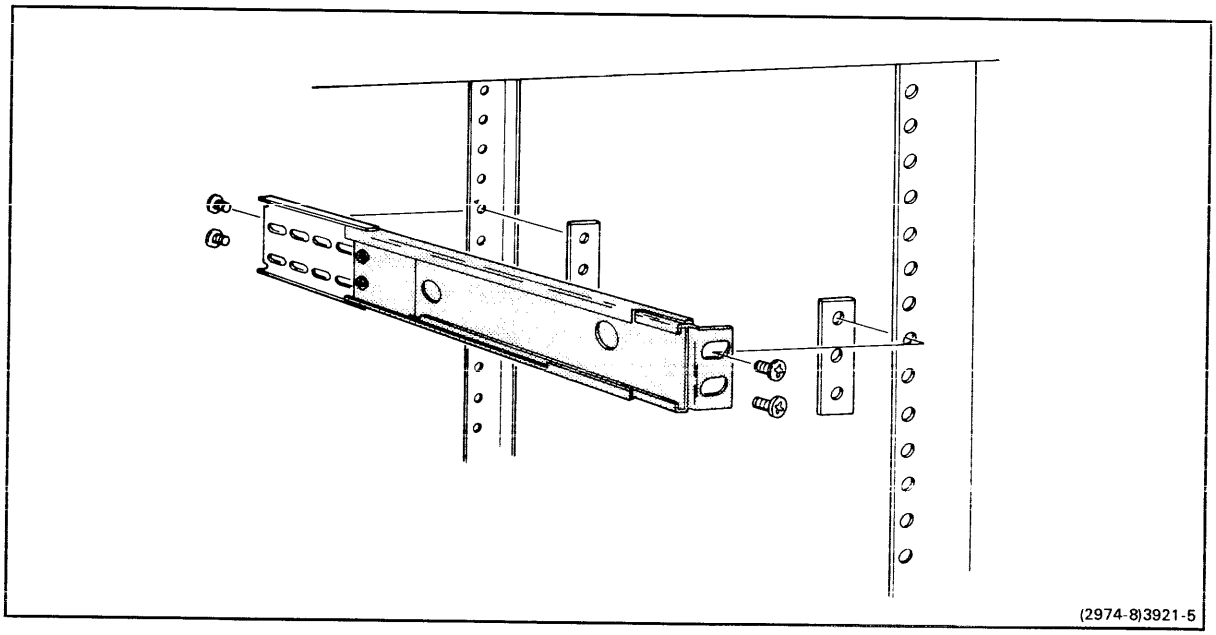


Fig. 3-3. Rack-mount guide orientation.

SELECTING THE PROPER PRIMARY VOLTAGE

The 8540 is configured to plug into the primary power source available at your work site. If, for some reason, you need to change power sources, use the following procedure:

1. Refer to Fig. 3-4. Notice the small plate near the center of the 8540 rear panel. Using a Phillips screwdriver, remove the screws holding this cover plate.

2. Beneath the cover plate, you'll see two slide switches, marked "HI--LOW" and "115--230". These switches select high or low voltage operation for either 115 or 230 volts.

3. Set the switches to the voltage of the primary power source. (See Table 3-1 to determine correct settings.)

@

CAUTION

The fuse rating depends on the voltage selected. The proper fuse must be used.

4. Install a fuse with the proper rating in the line fuse holder. For 115 volt operation, use a 3AG, 8 amp, 250 volt, medium-blow (5 sec.) fuse. For 230 volt operation, use a 3AG, 4 Amp, 250 volt, medium-blow (5 sec.) fuse.

5. Replace the switch cover plate to indicate the new voltage settings.

Table 3-1
Primary Voltage Switch Selection

Primary Voltage	Switch S300 115--230	Switch S301 HI--LOW
90--110 Vac	115	LOW
108--132 Vac	115	HI
180--220 Vac	230	LOW
216--250 Vac	230	HI

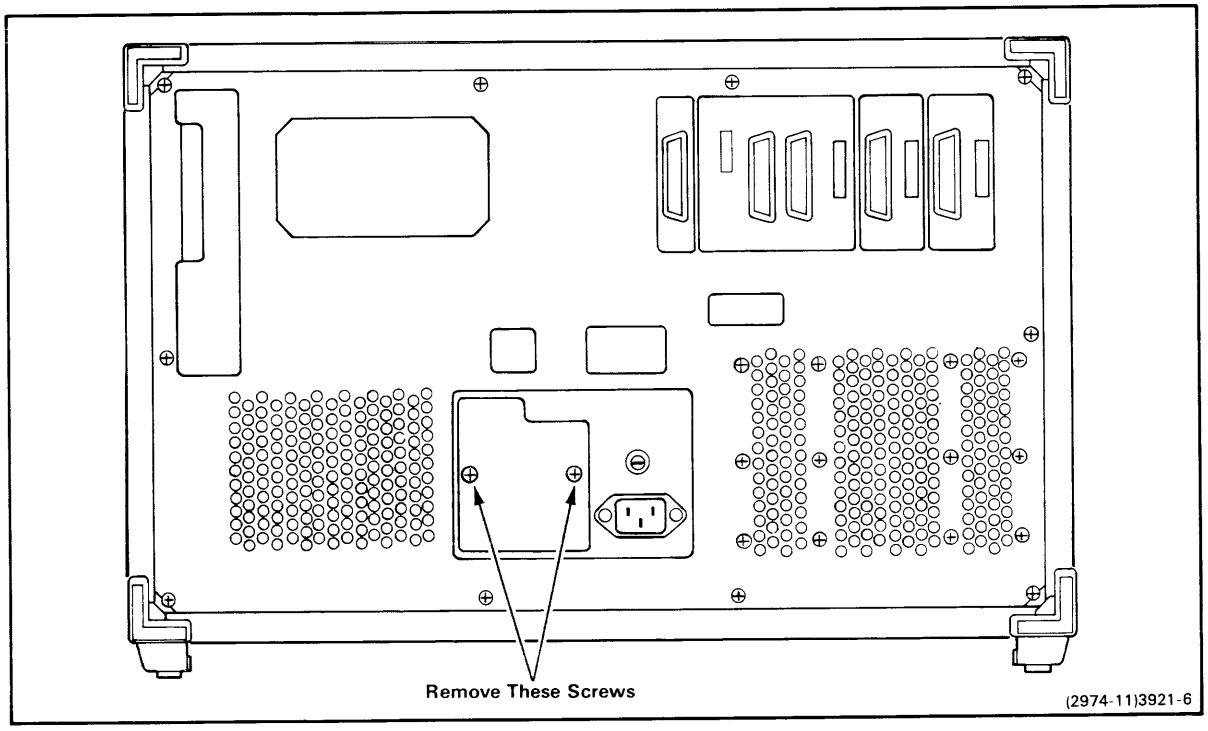


Fig. 3-4. 8540 primary voltage cover plate.

Section 4

8540 CONTROLS, CONNECTORS, AND INDICATORS

INTRODUCTION

This section briefly describes each of the 8540 controls, connectors, and indicators. In addition, the pin configurations for all rear panel connectors are also included. The 8540 front and rear panels are shown in Figures 4-1 and 4-2. The following descriptions of controls, connectors, and indicators are keyed to the circled numbers in Figures 4-1 and 4-2.

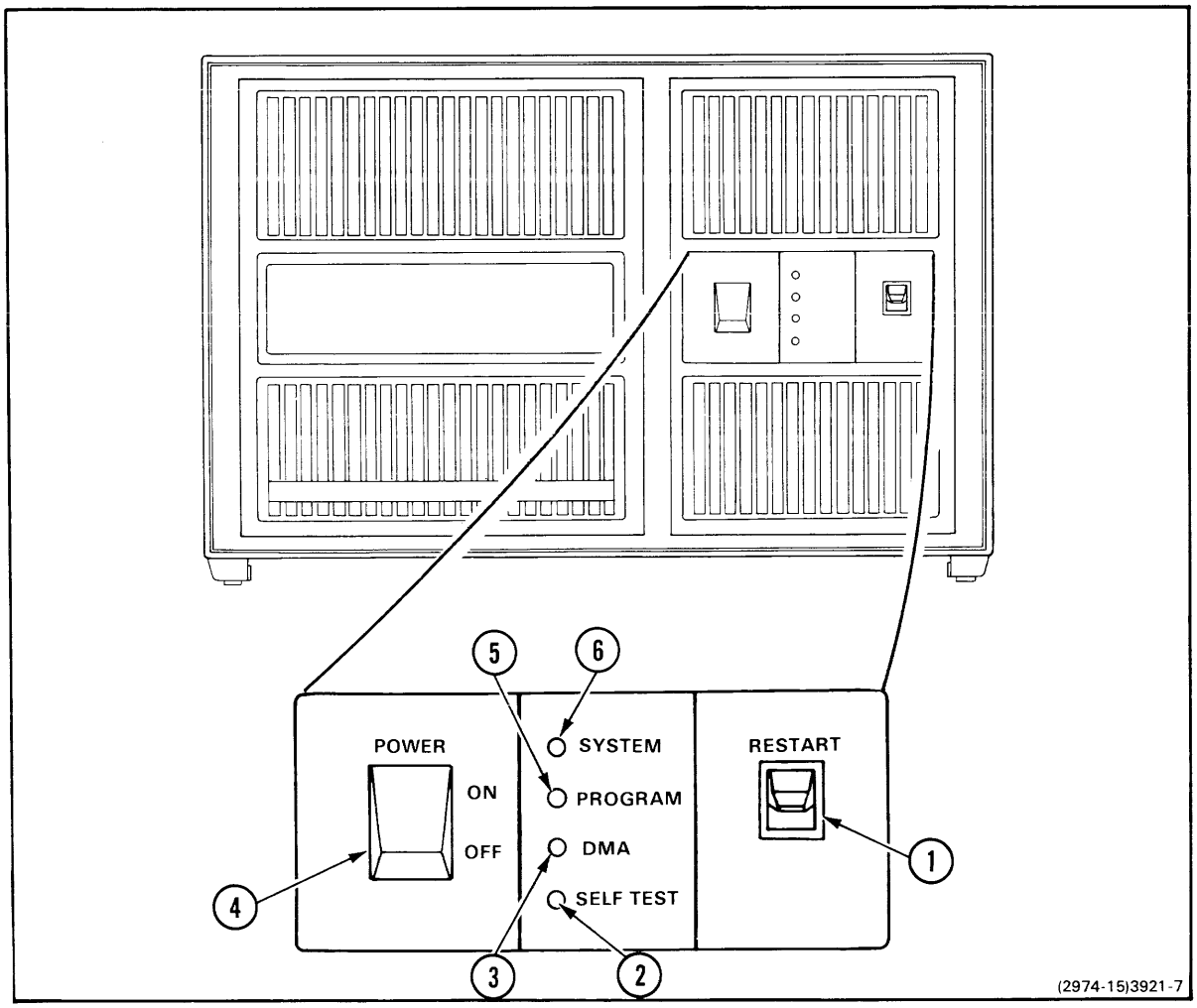


Fig. 4-1. 8540 front panel controls and indicators.

FRONT PANEL CONTROLS AND INDICATORS

1 RESTART

When this momentary-contact switch is toggled, the entire system is reset to its initial state. Note that the SELF TEST indicator should be lit after you toggle this switch.

2 SELF TEST

When this indicator is lit, the power-up diagnostics tests are running. If the indicator does not go out 5 seconds after power-up or re-booting, an error has been detected in a power-up test.

3 DMA

This indicator is lit when a direct memory access (DMA) operation is occurring.

4 POWER

This ON---OFF rocker switch controls primary power to the 8540.

5 PROGRAM

This indicator is lit when the emulator processor has control.

6 SYSTEM

This indicator is lit when the system processor has control.

REAR PANEL CONTROL AND CONNECTORS

7 LINE FUSE

This is the line fuse for the 8540. If the instrument is configured for 115 Vac, use a 3AG, 8 Amp, 250 Volt, medium-blow (5 sec.) fuse. If the instrument is configured for 230 Vac, use a 3AG, 4 Amp, 250 Volt, medium-blow (5 sec.) fuse.

8 PRIMARY POWER PLUG

This is the primary power supply plug for the 8540. Only the line voltage indicated by the voltage source cover plate should be connected.

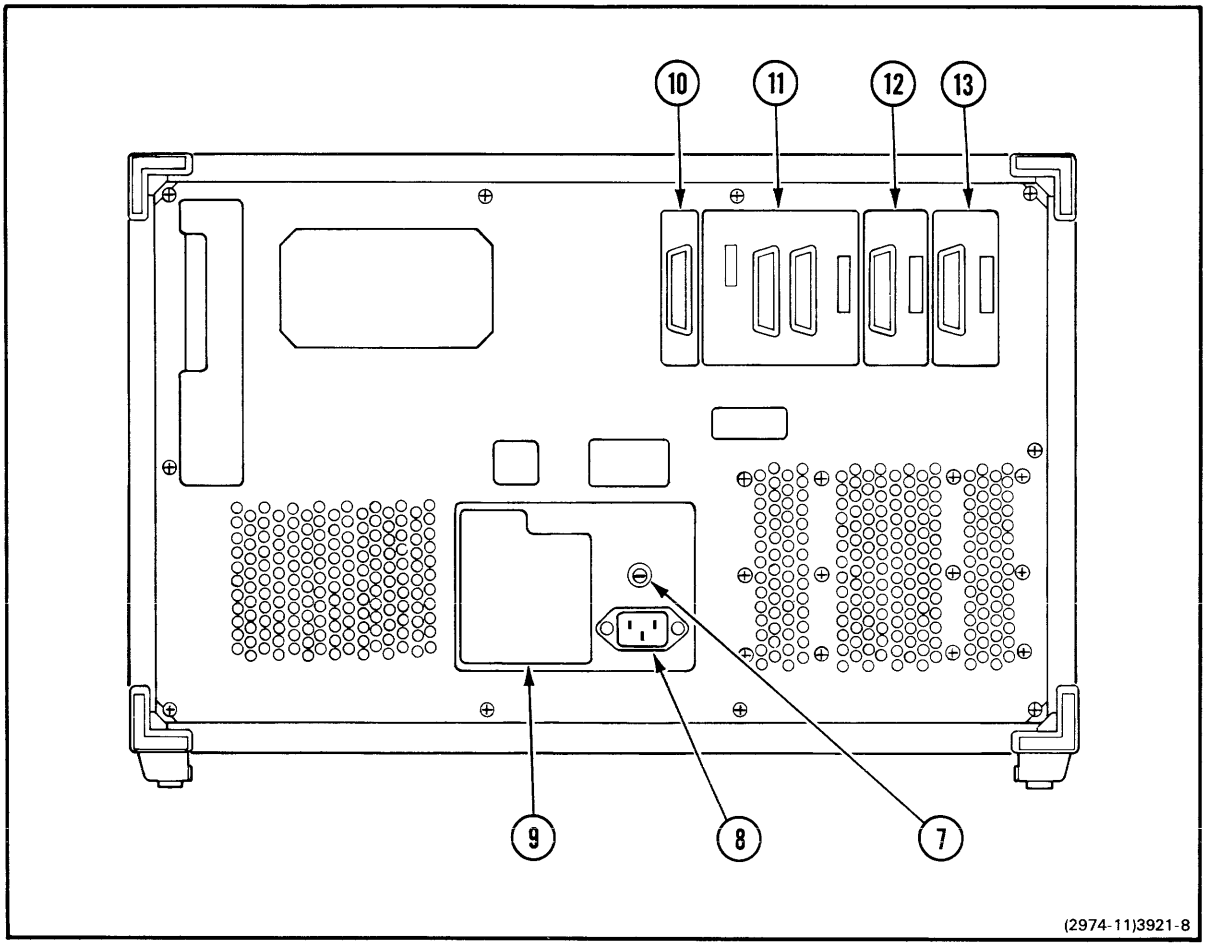


Fig. 4-2. 8540 rear panel control and connectors.

9 PRIMARY VOLTAGE SOURCE

The primary voltage source for an 8540 is selected at the factory with two switches: S300 and S301. A cover plate on the rear panel of the instrument indicates which of four possible voltage sources is selected. To change the voltage source, remove this cover plate and change the settings of the two-position switches. One switch, S300, selects 115 Vac or 230 Vac and a second switch, S301, selects a high or low range within 115 Vac or 230 Vac. If you change the voltage source, be certain that your instrument has the proper fuse for the new configuration. Then, replace the cover plate to indicate the new setting. Table 4-1 lists the voltage ranges for the switch positions.

Table 4-1
Primary Voltage Switch Selection

Primary Voltage	Switch S300 115--230	Switch S301 HI--LOW
90--110 Vac	115	LOW
108--132 Vac	115	HI
180--220 Vac	230	LOW
216--250 Vac	230	HI

10 HSI Port

J100 is the High-Speed Serial Interface (HSI) Port. The HSI Port is a modified RS-422 compatible serial interface designed to communicate with a data storage unit such as the TEKTRONIX 8560 Multi-User Software Development System or equivalent. This port operates only at 153.6K baud. Table 4-2 lists the pin configuration of J100.

Table 4-2
HSI Port -- J100 Pin Configuration

Pin No.	HSI Port J100 25-Pin Male
1	Shield
2	TX
3	RX
4	RTS
5	CTS
6--9	------
10	RTS'
11	TX'
12	RX'
13	DTR'
14--19	------
20	DTR
21--24	------
25	CTS'

11 REMOTE Port

J101 and J102 form the Remote Communications Port. This port is used to interface the 8540 with a general-purpose host computer. The port is also designed to interface the 8540 with a telephone modem. Both the male and female connectors of this port are RS-232-C compatible. The

Remote Port has two switches associated with it: MODE SELECT switch and BAUD switch. The BAUD switch selects one of eight baud rates. See Fig. 4-3. The MODE SELECT switch selects one of four operating modes. Table 4-3 lists the four operating modes. Table 4-4 lists the pin configurations for connectors J101 and J102.

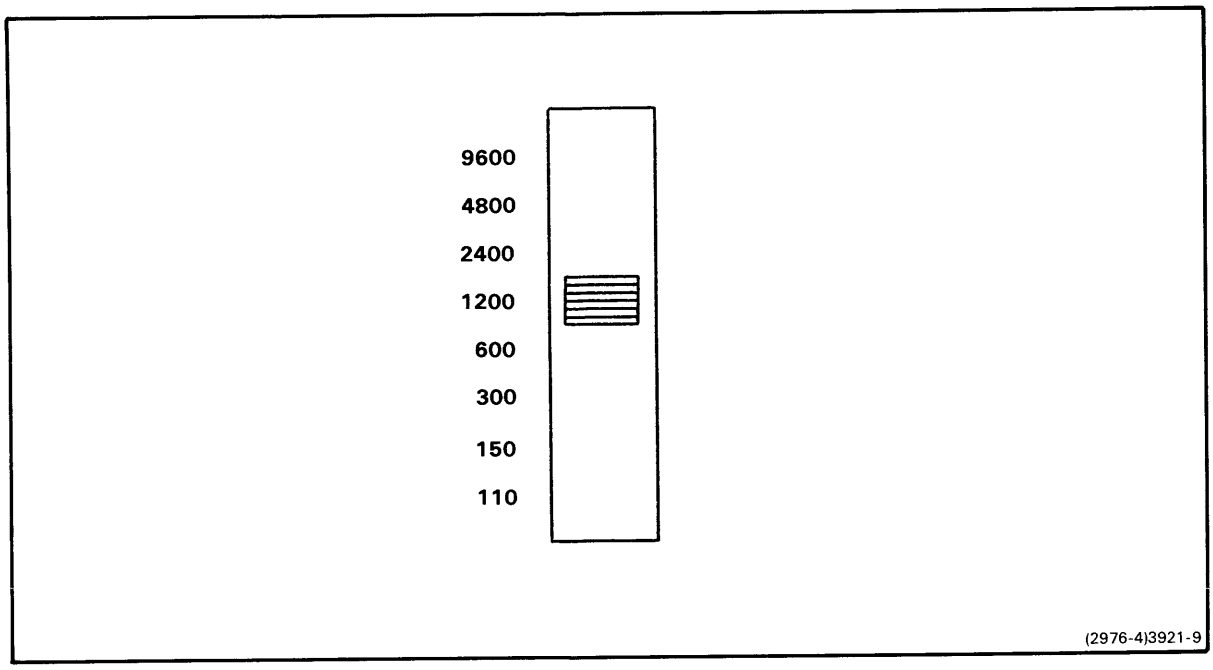


Fig. 4-3. Baud rate switch.

Table 4-3
MODE SELECT Switch
Remote Port Operating Modes

Switch Setting	RS-232-C Function
CNTL(L)	No Control
DTE1	DTE with CTS control
DTE2	DTE with DSR control
DCE	DCE with control

12 AUXILIARY Port

J103 is the Auxiliary Port. This port provides communications to and from auxiliary equipment, such as a line printer. The Auxiliary Port is an RS-232-C compatible port with a switch-selectable baud rate. In addition, a jumper-selectable external baud rate is also available on pin 17 of J103. The pin configuration for the Auxiliary Port is listed in Table 4-4. The baud rate switch is the same as that shown in Fig. 4-3.

13 TERMINAL Port

J104 is the Terminal Port. This RS-232-C compatible port with a switch-selectable baud rate provides a communications interface between the 8540 and the system terminal. The pin configuration for the Terminal Port is listed in Table 4-4. Figure 4-3 shows the baud rate switch settings.

Table 4-4
Pin Configurations for RS-232-C Compatible Ports

	Remote Port		Auxiliary Port	Terminal Port
Pin No.	J101 25-Pin Male	J102 25-Pin Female	J103 25-Pin Female	J104 25-Pin Female
1	Shield	Shield	Shield	Shield
2	TX	TX	TX	TX
3	RX	RX	RX	RX
4	RTS	RTS	RTS	RTS
5	CTS	CTS	CTS	CTS
6	DSR	DSR	DSR	DSR
7	LOGIC GND	LOGIC GND	LOGIC GND	LOGIC GND
8	DCD	DCD	DCD	DCD
9--16	------	------	------	------
17	------	------	EXT CLK	------
18--19	------	------	------	------
20	DTR	DTR	DTR	DTR
21--25	------	------	------	------

@

Section 5

8540 VERIFICATION

INTRODUCTION

Thus far, you have unpacked the 8540, prepared it for operation, and become somewhat familiar with the front panel controls and the rear panel connectors. In this section, we'll present a step-by-step procedure for verifying the operation of the 8540. We will also present some procedures to follow if an error is detected during the verification process. The 8540 is verified on a stand-alone basis, with only the system terminal attached to the 8540. The following information is included in this section:

- Attaching a terminal to the 8540
- Applying power to the 8540
- 8540 diagnostic tests
- 8540 system verification procedure
- What to do if an error is detected

ATTACHING A TERMINAL TO THE 8540

The upper right corner of the 8540 rear panel contains five serial data cable connectors for connecting peripheral equipment. See Fig. 5-1. The rightmost connector, labeled TERMINAL and J104, is used to attach the system terminal. The TERMINAL connector is RS-232-C compatible, and will accept most terminal data cables.

TERMINAL PORT SPECIFICATIONS

The TERMINAL port is a 25-pin female connector. The peripheral specifications and the RS-232-C signals used by the 8540 are listed in Table 2-13, in Section 2 of this manual. If your terminal uses a different signal arrangement, a "null" modem may have to be built to adapt your terminal to the 8540. If a TEKTRONIX CT 8500, 4024 or 4025 terminal is used, a null modem is not required.

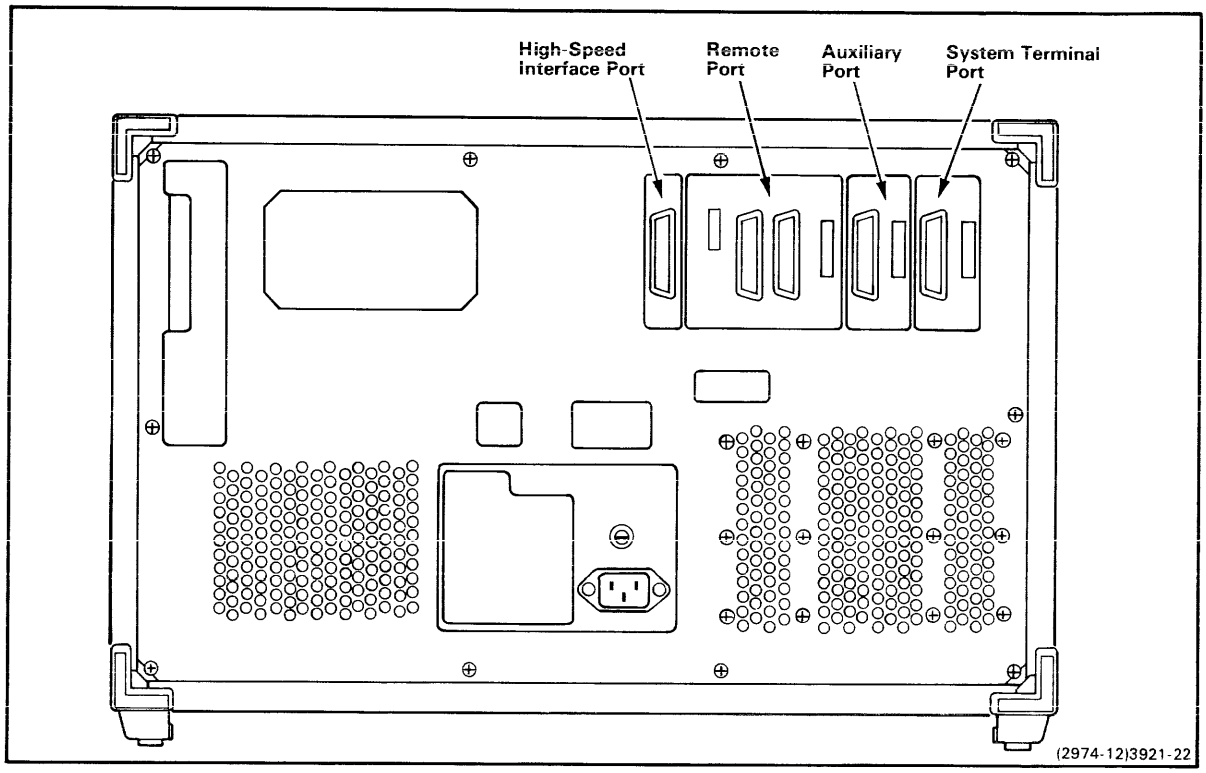


Fig. 5-1. Connectors for peripheral equipment.

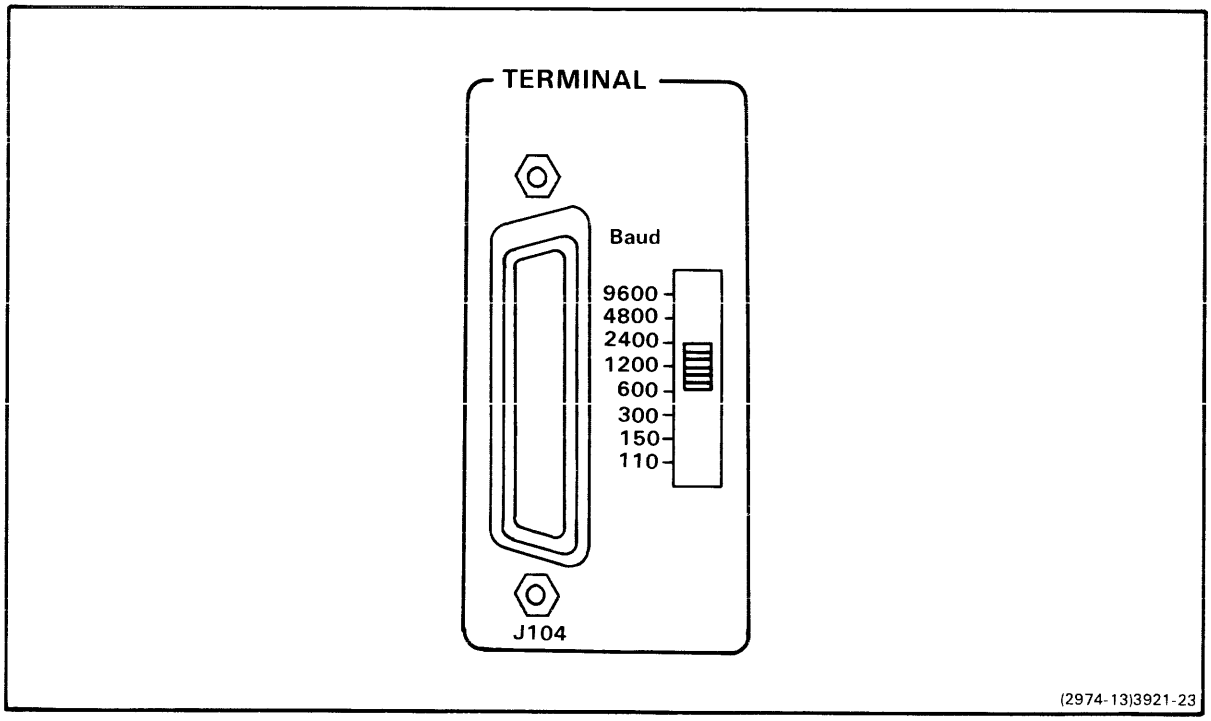


Fig. 5-2. Baud rate switch.

BAUD SELECTION

Figure 5-2 shows the baud rate switch, which is located to the right of the TERMINAL connector. Move the slide switch to the highest baud rate your terminal will accommodate. Make sure that the 8540 and terminal are both set to the same baud rate.

APPLYING POWER TO THE 8540

You are now ready to attach the power cord and apply primary power to the 8540.

CAUTION

As a precautionary step, make sure that the POWER switch on the 8540 front panel is OFF. Also make sure that the voltage indicated by the voltage source cover plate is the same as your primary voltage source. If it is not, refer back to Section 3 of this manual for information on how to select the proper primary voltage.

Attach the power cord to the rear of the 8540. Connect the other end of the power cord to the primary voltage source output plug.

You are now ready to verify that the 8540 is operational.

8540 DIAGNOSTIC TESTS

Two separate diagnostic test programs must be successfully executed to verify the 8540 system. These test programs are:

- power-up diagnostics
- ROM-resident diagnostics

POWER-UP DIAGNOSTICS

The power-up diagnostic tests are run automatically during power-up or restart conditions. These tests verify the circuitry within the 8540 that is required to boot and transfer the operating system from ROMs into the 8540's system memory. If the power-up test are passed, the operating system is automatically booted and the terminal displays the following message:

```
8540 BOOT Vx.x

(User start-up processing message from $STARTUP string
 goes here.  This message may or may not occur.)

OS/40 Vx.x(xxxx-xx) 12 OCT 1981   Copyright (c) 1981 Tektronix, Inc.

>
```

Power-Up Errors

Two types of errors can occur while the power-up diagnostics are running: fatal and non-fatal.

Fatal Error

A fatal error occurs if a fault is encountered that prohibits the ROM-resident diagnostics from running or prevents the operating system from booting. If a fatal error occurs, the test is suspended and the diagnostics branch to the Critical Function Monitor (CFM).

An error code is also displayed on three sets of LEDs: one set of five LEDs on the System Controller board, one set of five LEDs on the System RAM board, and one LED on the Front Control Panel labeled SELF TEST.

Non-Fatal Error

A non-fatal error occurs if a fault is detected in any part of the system that would not prohibit running the ROM-resident diagnostics. If a non-fatal error occurs, the ROM-resident diagnostics are automatically loaded and the diagnostic menus appear on the system terminal.

Critical Function Monitor (CFM)

The Critical Function Monitor (CFM) is automatically entered if a fatal error is encountered when running the power-up tests. The CFM provides a limited troubleshooting capability when the system cannot boot or run the ROM-resident diagnostics. The CFM contains several test routines and a limited set of user commands that are entered from the system terminal. A detailed description of the CFM and its use is contained in the 8540 Integration Unit Service Manual.

ROM-RESIDENT DIAGNOSTICS

The ROM-resident diagnostics provide the user with a means of verifying system performance, and a tool for troubleshooting in the event that a failure is detected during the running of any test. These diagnostics run automatically after being initiated by the user. Individual tests may also be executed by the user.

The ROM-resident diagnostics are menu-driven, which provide a friendly and easy-to-use interface with the user.

The 8540 Integration Unit Service Manual contains a detailed explanation of the ROM-resident diagnostics and how they are used.

8540 SYSTEM VERIFICATION PROCEDURE

The following procedure will step you through the power-up sequence and system verification. It is helpful to first read through this procedure before you start.

Procedure

1. Turn on the 8540 by pushing the 8540 POWER switch to the ON position.

2. As soon as the POWER switch is in the ON position, the front panel LEDs labeled SYSTEM and SELF TEST will light.

3. After a few seconds, the LED marked DMA will flash very briefly, and then the SELF TEST lamp will go out.

4. At this time, the system terminal will display the following boot message:

```
8540 BOOT Vx.x

(User start-up processing message from $STARTUP string
 goes here.  This message may or may not occur.)

OS/40 Vx.x(xxxx-xx) 12 OCT 1981   Copyright (c) 1981 Tektronix, Inc.

>
```

5. This completes the 8540 power-up sequence. Continue with this procedure for system verification.

6. Enter the following command on the system terminal.

```
> SELECT DIAGS
```

7. The ROM-resident diagnostics will be loaded and the following information is displayed on the system terminal:

```
*********************************************
*                                           *
*  TEKTRONIX INC.                           *
*  8540 ROM-RESIDENT DIAGNOSTIC SYSTEM      *
*  VERSION X.X                              *
*  Copyright (c) 1981 Tektronix, Inc.       *
*                                           *
*********************************************


                  RUN MODE MENU

1 - AUTOMATIC MODE          ***** Default *****
2 - SELECT MODE

Type mode :
```

8. Press the RETURN key on the terminal (or press 1 and RETURN keys). This selects the default or Automatic Mode. The Automatic Mode Menu is displayed below the Run Mode Menu, as follows:

```
*******************************************
*                                         *
*  TEKTRONIX INC.                         *
*  8540 ROM-RESIDENT DIAGNOSTIC SYSTEM    *
*  VERSION X.X                            *
*  Copyright (c) 1981 Tektronix, Inc.     *
*                                         *
*******************************************


                RUN MODE MENU

1 - AUTOMATIC MODE          ***** Default *****
2 - SELECT MODE

Type mode :


                AUTOMATIC MODE MENU

1 - AUTOMATIC SYSTEM VERIFICATION        ***** Default *****
2 - RUN ALL TESTS CONTINUALLY
3 - RUN SPECIFIED TESTS

Type mode :
```

9. Press the RETURN key again, and the Display Option menu is displayed below the Automatic Mode Menu, as follows:

```
*********************************************
*                                           *
*  TEKTRONIX INC.                           *
*  8540 ROM-RESIDENT DIAGNOSTIC SYSTEM      *
*  VERSION X.X                              *
*  Copyright (c) 1981 Tektronix, Inc.       *
*                                           *
*********************************************


                RUN MODE MENU

1 - AUTOMATIC MODE          ***** Default *****
2 - SELECT MODE

Type mode :


                AUTOMATIC MODE MENU

1 - AUTOMATIC SYSTEM VERIFICATION        ***** Default *****
2 - RUN ALL TESTS CONTINUALLY
3 - RUN SPECIFIED TESTS

Type mode :


                 DISPLAY OPTION

1 - TERMINAL                             ***** Default *****
2 - TERMINAL + 8540 PRINTER
3 - NO DISPLAY

Type Option :
```

10. Press the RETURN key again. This starts the execution of the Automatic System Verification tests. No further intervention is required.

11. Various TEST RUNNING messages are displayed as the verification tests are executing. After approximately five minutes, if no failures are detected, the tests are completed, and the following message is displayed:

    SYSTEM VERIFICATION PASSED

    NOTE

    The basic 8540 unit and all options installed in the 8540 are automatically tested during the system verification tests.

    If a failure is detected during the running of the tests, a DIAGNOSTIC FAILURE message is displayed and the tests continue. When the tests are completed this message is displayed:

    SYSTEM VERIFICATION FAILED

12. This completes the 8540 system verification procedure. If the system failure message is displayed, refer to the following paragraph.

WHAT TO DO IF AN ERROR IS DETECTED

If the SYSTEM VERIFICATION FAILED message is displayed, the diagnostics found a fault in the 8540 unit or in one of the options installed. In that case, refer to the 8540 Integration Unit Service Manual. The service manual contains information on performing exhaustive diagnostic tests. These tests are designed to isolate faults to a board level, and in many instances to the faulty device.

Section 6

8540 SYSTEM CONFIGURATIONS

INTRODUCTION

The 8540 is a distributed hardware/software integrated workstation. The 8540 operates in conjunction with a host computer. The 8540 can be configured with several different types of host computers. The system configurations are dependent on:

- o the type of host computer.
- o the location of the system terminal.
- o the distance between the 8540 and the host computer.
- o the software/hardware interface between the 8540 and the host computer.

This section describes the host computer configurations and the interface requirements for each configuration. The following host configurations are discussed:

1. 8540/General Host

   The 8540 can communicate with any host computer that supports asynchronous RS-232-C protocol. The host computer software for formatting data and driving the communication line to the 8540 must be provided by the user.

2. 8560/8540 System

   The TEKTRONIX 8560 Multi-User Software Development Unit is a multi-user unit based on the DEC 11-23 computer. The 8560 supports up to eight hardware workstations (8540s) or terminals. The system terminal may be connected to the 8540 or directly to the 8560. Tektronix, Inc. provides extensive software development tools (assemblers and compilers) that run on the 8560.

GENERAL HOST CONFIGURATION

The 8540 can communicate with any host computer that is compatible with asynchronous RS-232-C protocol. The host computer must also provide software support for the 8540 interface. Figure 6-1 shows the interconnecting cables between the 8540 and the general host computer.

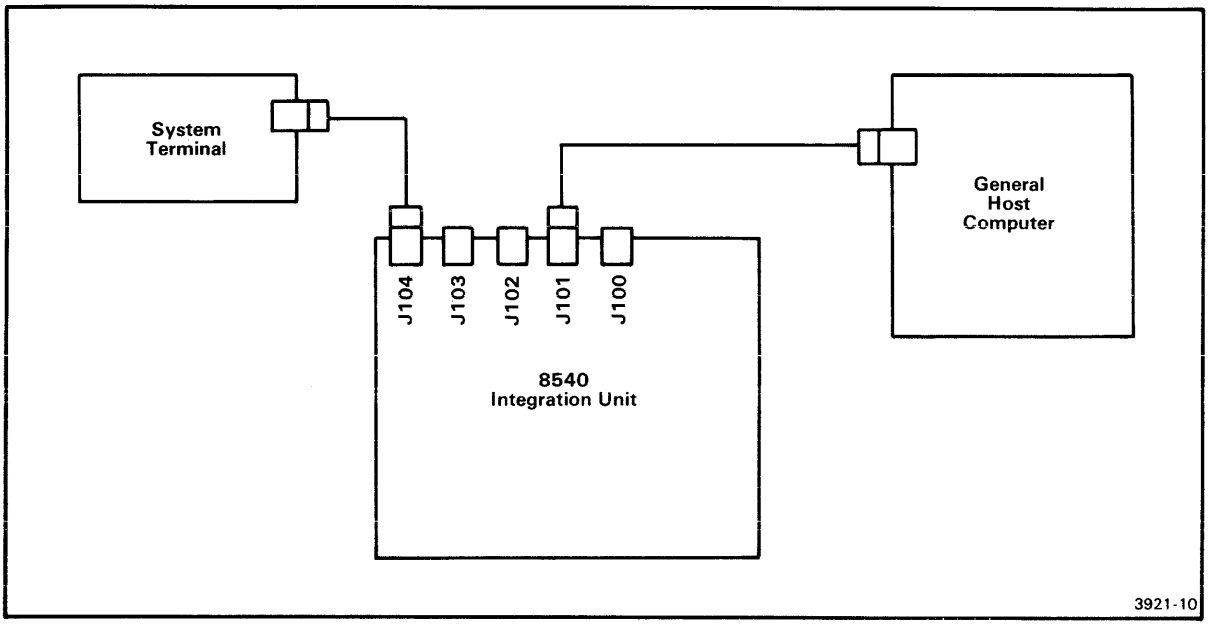


Fig. 6-1. General host configuration.

HOST REQUIREMENTS

When a general purpose computer is used as the host to the 8540 IU, the following requirements are imposed on the host computer:

1. The host computer is used to edit, compile and link files using host-provided software.

2. The files must be converted to TEKHEX format, unless a linker or compiler is used that provides TEKHEX format.

3. The files are then downloaded to the 8540's Program Memory.

4. Once the downloading is complete, the host computer may be disconnected from the 8540.

HOST SOFTWARE INTERFACE REQUIREMENTS

The 8540 provides no software support for the interface to the general host computer. The software interface must be in TEKHEX format. Refer to the 8540 System Users Manual for more information about; uploading, downloading, TEKHEX formatting, and Symbol Table formatting.

HOST HARDWARE INTERFACE REQUIREMENTS

The physical interface between the 8540 and the general host computer is via the REMOTE communications port on the 8540 rear panel. This port provides RS-232-C compatible, asynchronous, ASCII communications at baud rates up to 9600. Figure 6-1 shows the interconnections between the 8540 and the host computer.

The REMOTE port has two 25-pin connectors: one male (J101) and one female (J102). Only one connector can be used at a time. Connect the female end of the RS-232-C interface cable to J101 (DTE connector) on the 8540 rear panel. Set the MODE SELECT switch, adjacent to J101, to DTE1. Connect the other end of the cable to the host computer. Refer to Section 2, Tables 2-7 through 2-11 of this manual, for the pin configurations and peripheral interface requirements for J101 and J102. Figure 6-2 shows the RS-232-C interface cable between the 8540 and general host computer.

SYSTEM TERMINAL REQUIREMENTS

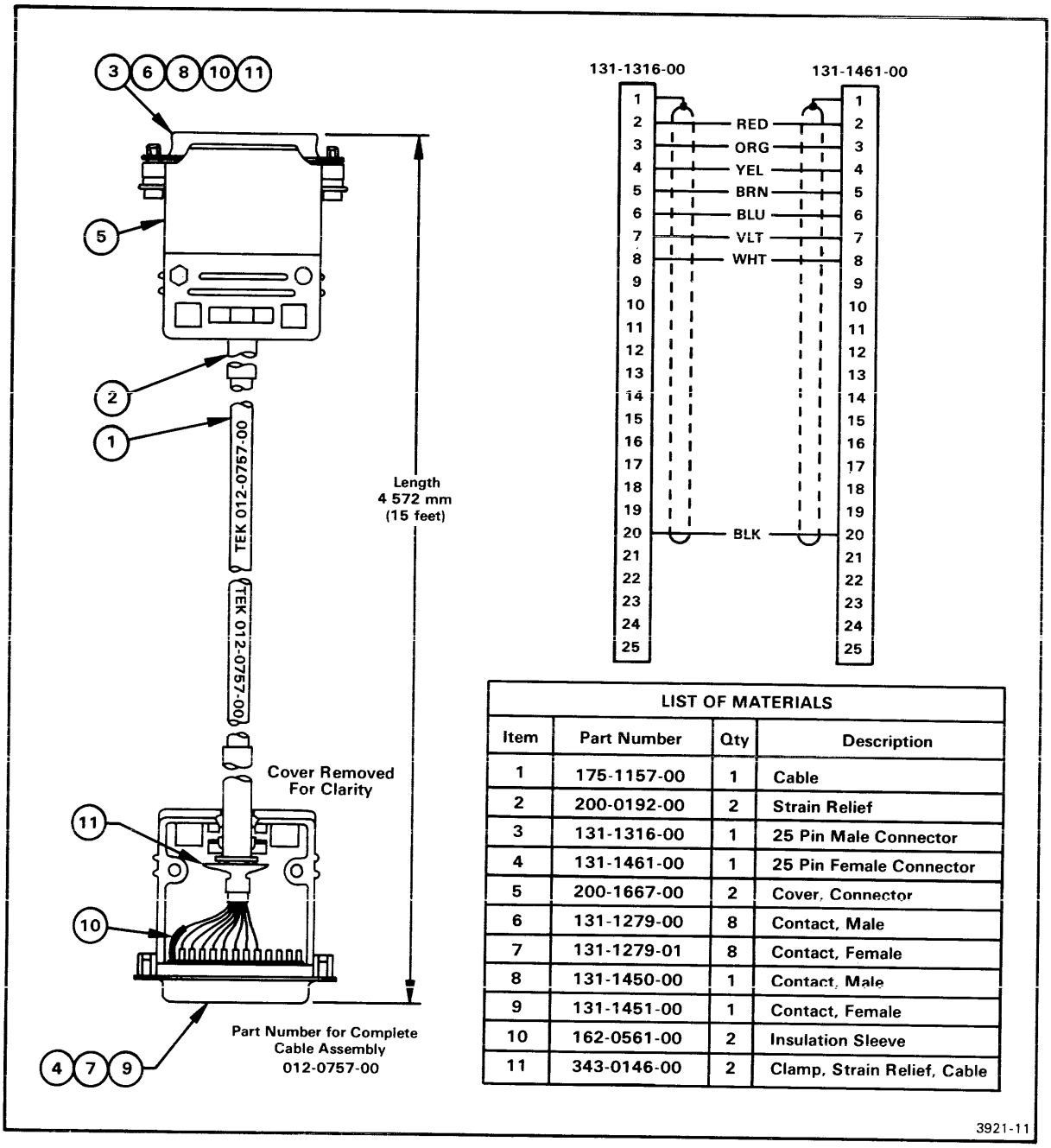
Figure 6-1 shows the system terminal connected to the 8540.

Terminal Connected to 8540

When the terminal is connected to the 8540, the terminal transparent mode of operation is used. In this mode the user can:

- use the host-based screen-oriented editors.
- manipulate files in the host computer.
- download files to the 8540 (provided that the files have been converted to TEKHEX format).

The terminal communicates with the host computer as if the 8540 wasn't really there. All data received by the 8540 from the terminal is transferred to the host computer and back, without being altered by the 8540. This interface is so thoroughly transparent no character or sequence of characters can exit this operating mode. Therefore, to exit this mode the user must physically press the RESET switch on the front of the 8540.



LIST OF MATERIALS

Item	Part Number	Qty	Description
1	175-1157-00	1	Cable
2	200-0192-00	2	Strain Relief
3	131-1316-00	1	25 Pin Male Connector
4	131-1461-00	1	25 Pin Female Connector
5	200-1667-00	2	Cover, Connector
6	131-1279-00	8	Contact, Male
7	131-1279-01	8	Contact, Female
8	131-1450-00	1	Contact, Male
9	131-1451-00	1	Contact, Female
10	162-0561-00	2	Insulation Sleeve
11	343-0146-00	2	Clamp, Strain Relief, Cable

Fig. 6-2. RS-232-C interface cable.

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The terminal is connected to the TERMINAL port (J104) of the 8540. This port is an RS-232-C 25-pin female connector. Refer to Section 2, Table 2-13 of this manual, for the pin configuration and peripheral interface requirements for J104. Figure 6-2 shows the RS-232-C interface cable between the system terminal and the 8540.

8560/8540 SYSTEM

The 8560 Multi-User Software Development Unit is a multi-user microcomputer design unit. The 8560 is designed to operate with up to eight work stations. A work station is an 8540 or a terminal. Up to eight 8540's and terminals can be connected to the 8560, in any combination. Figure 6-3 shows the interconnecting cables between the 8560, 8540, and system terminal.

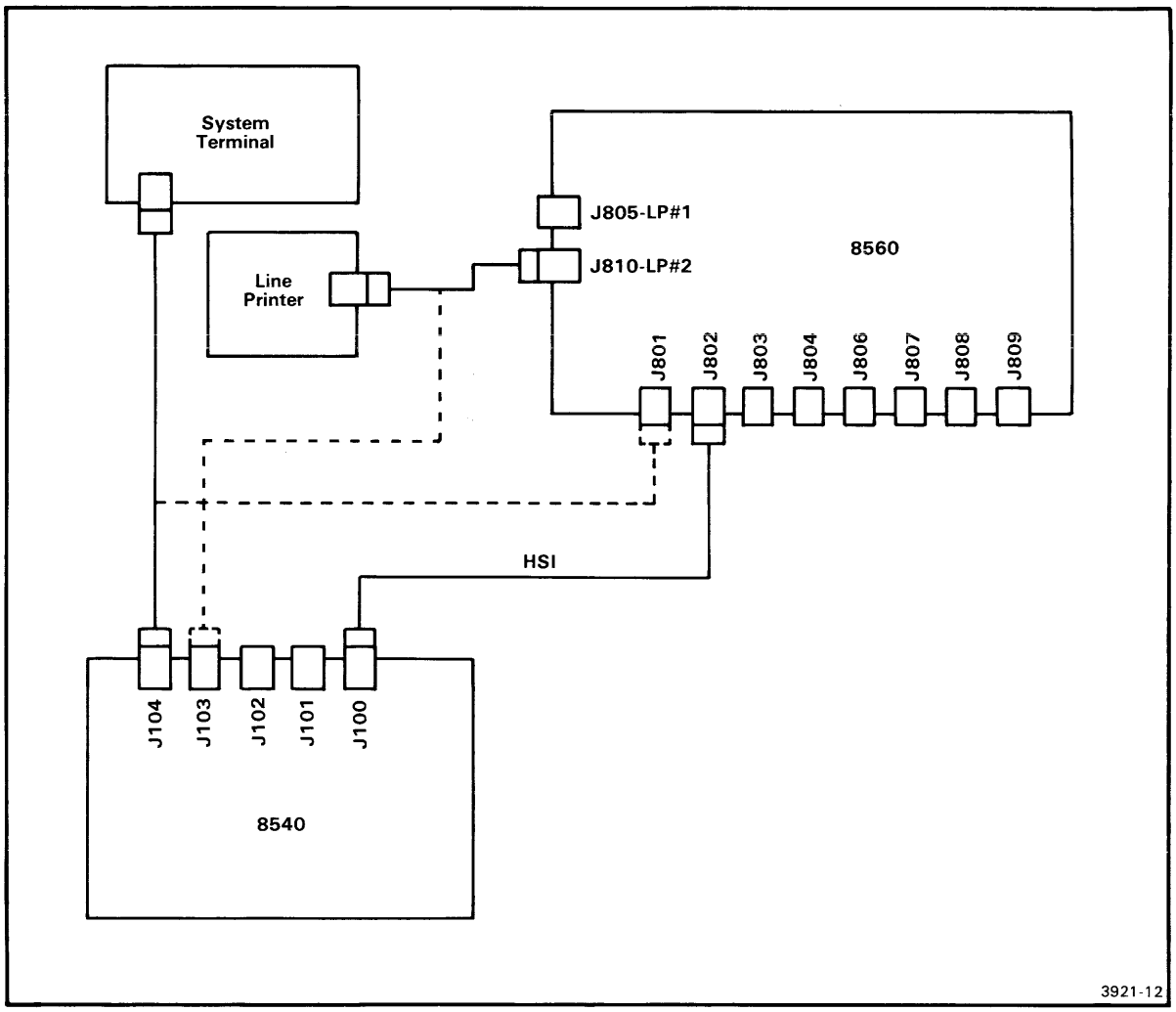


Fig. 6-3. 8560/8540 System.

SOFTWARE INTERFACE REQUIREMENTS

The operating system for the 8560/8540 System is based on the DEC 11-23 computer. The complete software package is provided with the 8560 and 8540 units. Refer to the appropriate System Users Manual for information regarding system commands and operation.

HARDWARE INTERFACE REQUIREMENTS

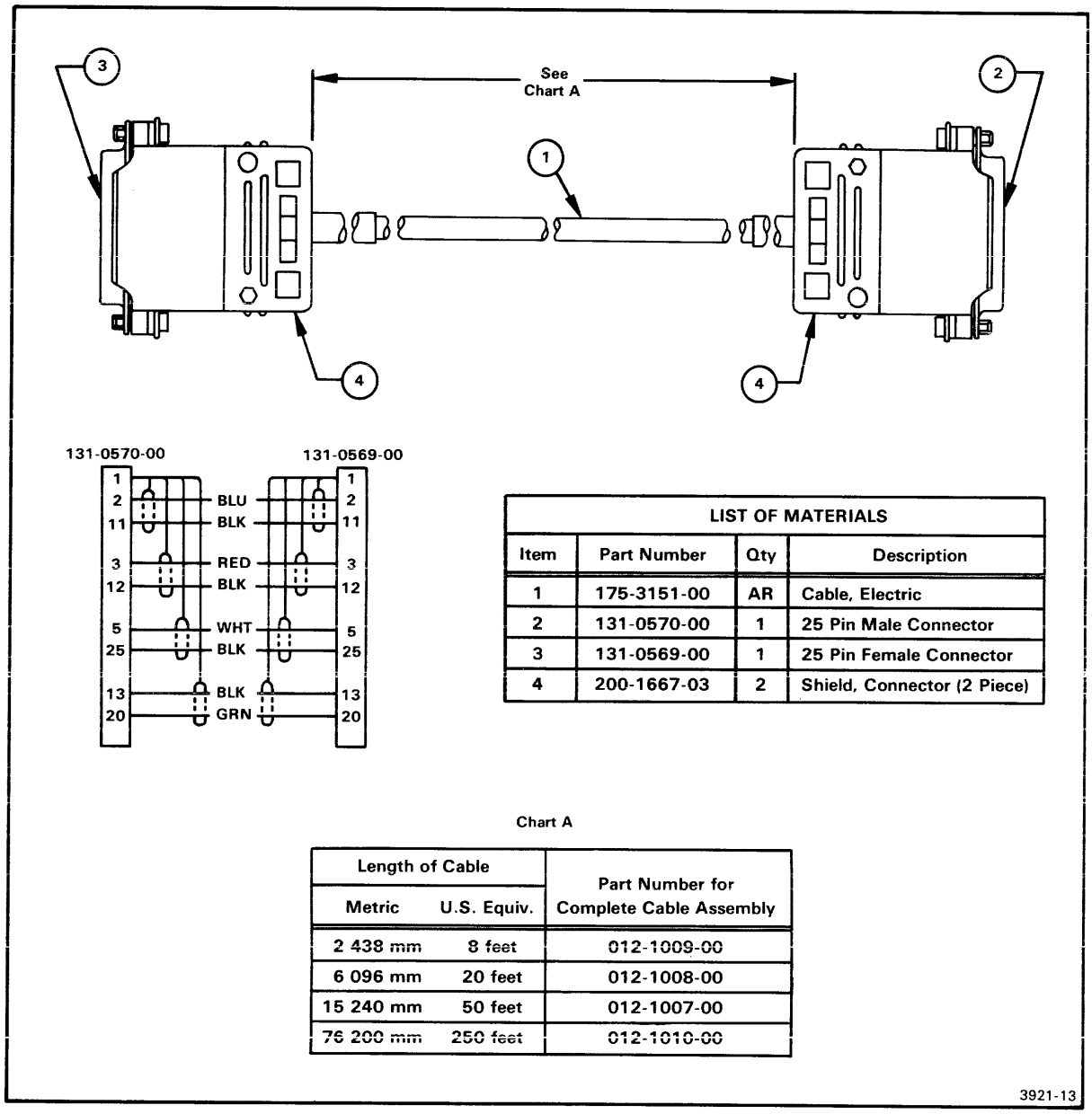
Figure 6-3 shows the interconnections between the 8540 and the 8560. The standard hardware interface between the 8540 and the 8560 is the TEKTRONIX High-Speed Serial Interface (HSI). This interface is RS-422 compatible and transfers data at a rate of 153.6K baud, which is 16 times faster than the fastest RS-232-C baud rate of 9600 baud. The maximum recommended HSI cable length between the 8540 and 8560 is 1,000 feet (304 m). Four standard lengths of interface cable are available as optional accessories to the 8540. These cables may be ordered through your local Tektronix Field Office or representative. Refer to Fig. 6-4 for a drawing of the RS-422 interface cable between the 8540 and 8560. The four HSI Communications cables are as follows:

- 8 feet (2.4 m) --- 012-1009-00
- 20 feet (6.1 m) --- 012-1008-00
- 50 feet (15.2 m) --- 012-1007-00
- 250 feet (76.2 m) --- 012-1010-00

If your installation requires a cable length in excess of the 250 feet standard length, but less than the 1,000 feet (304 m) maximum length, You can fabricate a cable to your desired length. Refer to Fig. 6-4 for information on how the cable is assembled. The cable specifications and recommended source are listed in Table 6-1.

Table 6-1
Specifications for HSI Cable

Characteristics	Description
Design Specifications	Shall meet or exceed the specifications of EIA RS-422-A.
Length of Cable	The HSI cable should not exceed the recommended maximum length of 1,000 feet (304 meters).
General Description	The cable shall consist of four insulated twisted pairs of wires, 24 AWG stranded, each pair individually shielded by foil and jacketed overall by PVC.
Shielding	Each pair of wires shall be individually shielded with aluminized mylar, 100% coverage.
Serving	Cable shall be served with a nylon fiber on 1.00 +/- .025 in. lay.
Drain Wires	Each twisted pair shall have a drain wire (19 strands of size 36 AWG tin coated copper). Overall size of drain wire is 24 AWG.
Nominal Resistance	The dc resistance of conductors---78.7 ohms/1000 meters (24 ohms/1000 feet. The dc resistance of individual shields---59.1 ohms/1000 meters (18 ohms/1000 feet).
Nominal Capacitance	Capacitance between conductors---41.0 pF/meter (12.5 pF/feet). Capacitance between one conductor and the other conductors connected to the shield ---72.5 pF/meter (22.0 pF/foot).
Recommended Source	Belden, Datalene cable, Type No. 19299 or equivalent.



LIST OF MATERIALS			
Item	Part Number	Qty	Description
1	175-3151-00	AR	Cable, Electric
2	131-0570-00	1	25 Pin Male Connector
3	131-0569-00	1	25 Pin Female Connector
4	200-1667-03	2	Shield, Connector (2 Piece)

Chart A

Length of Cable		Part Number for Complete Cable Assembly
Metric	U.S. Equiv.	
2 438 mm	8 feet	012-1009-00
6 096 mm	20 feet	012-1008-00
15 240 mm	50 feet	012-1007-00
76 200 mm	250 feet	012-1010-00

Fig. 6-4. RS-422 interface cable.

The HSI cable is connected to the HSI port (J100) of the 8540 as shown in Fig. 6-3. This port is a 25-pin female connector. Refer to Section 2, Table 2-6 of this manual, for the pin configuration and peripheral interface requirements for J100.

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SYSTEM TERMINAL REQUIREMENTS

Figure 6-3 shows the system terminal connected to either the 8540 or the 8560.

Terminal Connected to the 8540

When the terminal is connected to the 8540, the TERMINAL port (J104) is used. Refer to Section 2, Table 2-13 of this manual, for the pin configuration and peripheral interface requirements for J104. Figure 6-2 shows the RS-232-C interface cable.

Terminal Connected to the 8560

When the terminal is connected to the 8560, one of the RS-232/HSI ports (J801--J804 and J806--J809) is used. Each of these ports is capable of either RS-232-C or RS-422 terminations. Refer to your 8560 Installation Guide for information on how these ports are configured for either RS-232-C or RS-422 terminations.

OTHER PERIPHERAL REQUIREMENTS

Figure 6-3 shows a line printer connected to either the 8560 or the 8540. When the line printer is connected to the 8540, the AUXILIARY port (J103) is used. Refer to Section 2, Table 2-12 of this manual, for the pin configuration and peripheral interface requirements for J103. Figure 6-2 shows the RS-232-C interface cable. When the line printer is connected to the 8560, either connector LP #1 (J805) or LP #2 (J810) can be used. Refer to your 8560 Installation Guide for information on these ports.

RS-232-C INTERFACE REQUIREMENTS

Communications are also possible between the 8540 and 8560 via the REMOTE ports (J101 and J102) of the 8540. This is an RS-232-C compatible interface with a maximum baud rate of 9600. Refer to Section 2, Tables 2-7 and 2-11 of this manual, for the pin configurations and peripheral interface requirements for J101 and J102. Refer to your 8560 Installation Guide for information on configuring the 8560 RS-232/HSI ports for RS-232-C operation. The 8540 System Users Manual describes the use of the software commands, that establish and maintain communications over this interface.

Section 7

8540 CIRCUIT BOARD CONFIGURATIONS

INTRODUCTION

The circuit boards within the 8540 utilize jumpers and straps to reconfigure or change the function(s) of the circuit board. This section describes the jumpers and straps located on all standard circuit boards within the 8540. The use of each jumper and strap is described, along with the "normal" and alternate positions.

JUMPERS AND STRAPS

The following paragraphs define the kinds of jumpers and straps that are used on the standard circuit boards and describe how these connectors can select alternate functions.

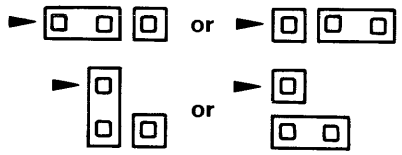
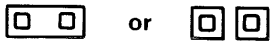
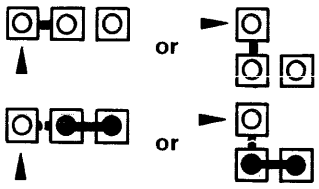
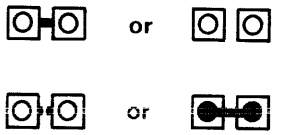
JUMPERS

In this manual, the term "jumper" refers to a small connector designed to fit across a jumper position. A "jumper position" consists of two square pins that can accommodate the placement of the jumper. Jumper positions are arranged on the circuit boards as single-position or two-position jumpers. Single-position jumpers have only two square pins: the jumper is either installed or removed. Two-position jumpers have three square pins, arranged in a straight line or "L" pattern. The jumpers may be installed on pins 1 and 2, 2 and 3, or removed. Table 7-1 shows the symbols used for jumpers in the circuit board configuration drawings that appear later in this section. Jumpers are designated with the prefix "J".

STRAPS

In this manual, the term "strap" refers to an ECB through-hole that may be bridged with a soldered wire to select an alternate function. A strap is also associated with a "cuttable run": an ECB run between two through-holes. The run must be cut before one of the through-holes can be strapped to a third through-hole. If there is a cuttable run at the location, it must be cut before the strap is bridged, to prevent system errors. Table 7-1 shows the symbols used for straps in the circuit board configuration drawings that appear later in this section. Straps are designated with the prefix "W".

Table 7-1
Symbols for Jumpers and Straps
Used on Circuit Board Configuration Drawings

Jumper/Strap Symbols	Usage
	These two-position jumpers show the jumper across pins 1 and 2 or across pins 2 and 3.
	This single-position jumper shows the jumper across the single jumper position or the jumper removed.
	These two-position straps show the cuttable runs between pins 1 and 2. The runs may be cut and the straps bridged across pins 2 and 3.
	These single-position straps show the through-holes with or without a cuttable run. The cuttable run may be cut or the through-holes may be bridged with a strap.

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SYSTEM CONTROLLER BOARD CONFIGURATION

Figure 7-1 shows the locations of jumpers and straps on the System Controller board, and the type of connector at each location. There are three jumpers and eight straps on the System Controller board. In addition, Fig. 7-1 shows the locations of a DIP switch (S1100) and LEDs associated with ROM-based diagnostics. Table 7-2 lists the jumper and strap configuration required for normal operation.

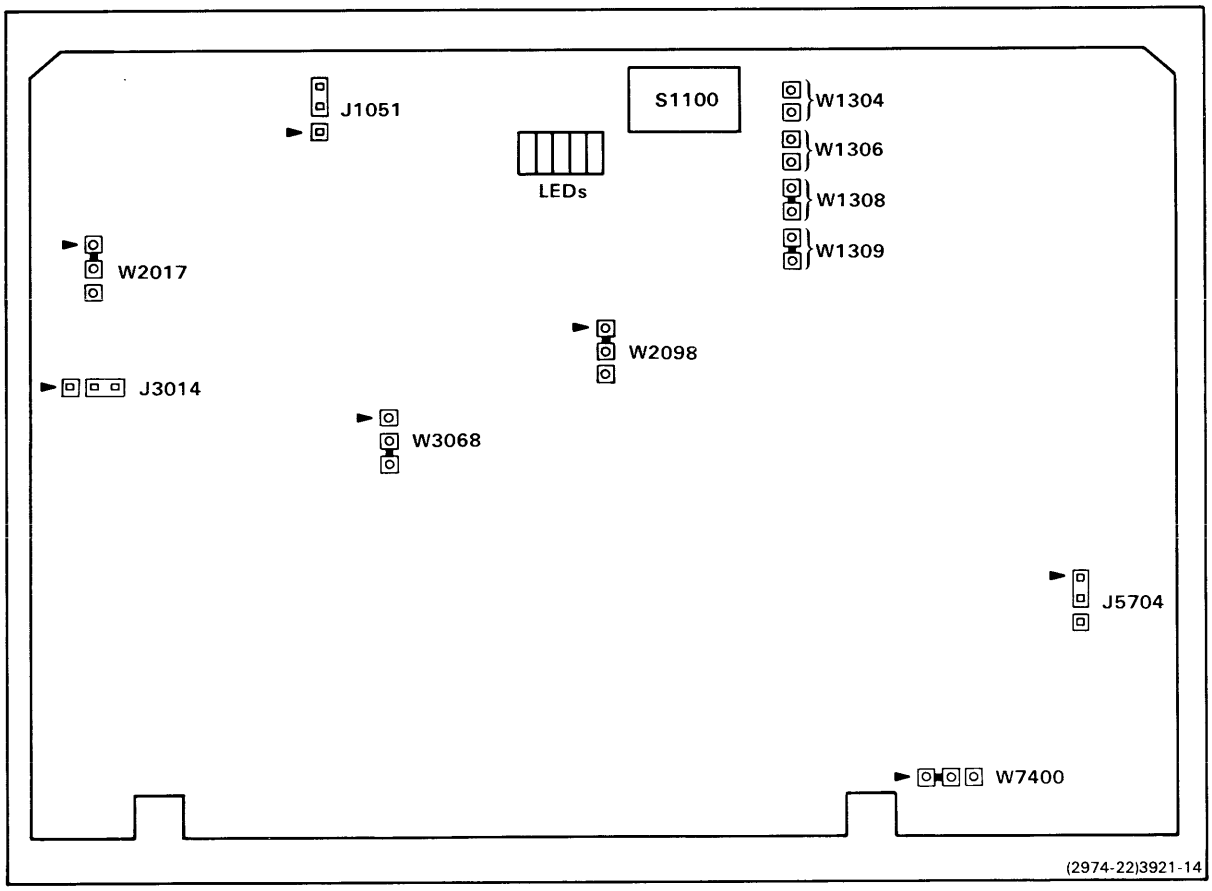

Fig. 7-1. System Controller board jumpers and straps.

Table 7-2
System Controller Board Normal Operating Configuration

Number	Jumper or Strap	Normal Operating Configuration
J1051	CPU Float Jumper	Jumper across pins 2 and 3
J3014	Forced Diagnostic Jumper	Jumper across pins 2 and 3
J5704	2650A Clock Jumper	Jumper across pins 1 and 2
W1304	Even/Odd Parity Strap	No change in original strapping
W1306	High-Speed Interface Strap	No change in original strapping
W1308	Stop Bit Select Strap	No change in original strapping
W1309	Parity Inhibit Strap	No change in original strapping
W2017	Bootstrap Limiting Strap	No change in original strapping
W2098	Direct Interrupt Strap	No change in original strapping
W3068	Mapping/Write Protect Strap	No change in original strapping
W7400	Line Grounding Strap	No change in original strapping
S1100	Diagnostics Mode Switch	Set the six switches to ON

2650A-1 CLOCK JUMPER

J5704 is the 2650A Clock Jumper. This two-position jumper selects either a 2 MHz System Clock or a 1.25 MHz System Clock. Pins 1 and 2 select 2 MHz. Pins 2 and 3 select 1.25 MHz. For normal operation, place the jumper across pins 1 and 2.

FORCED DIAGNOSTIC JUMPER

J3014 is the Forced Diagnostic Jumper. This two-position jumper forces the Diagnostic ROM on the bus, or allows software to select the Diagnostic or Boot ROMs. Pins 1 and 2 select only the Diagnostic ROM. Pins 2 and 3 select the Diagnostic or Boot ROMs. For normal operation, place the jumper across pins 2 and 3.

MAPPING/WRITE PROTECT STRAP

W3068 is the Mapping/Write Protect Strap. This two-position strap enables the Mapping/Write Protect function during normal operation. If the run between pins 2 and 3 is cut and a strap is placed between pins 1 and 2, the Mapping/Write Protect function is disabled.

CPU FLOAT JUMPER

J1051 is the CPU Float Jumper. This two-position jumper determines the state of the CPU READ(L) signal. If CPU READ(L) is high, the 2650A-1 can write to the system data bus. If CPU READ(L) is low, the 2650A-1 can read the system data bus. Pins 1 and 2 select a high on CPU READ(L). Pins 2 and 3 select a low on CPU READ(L). For normal operation, place the jumper across pins 2 and 3.

LINE GROUNDING STRAP

W7400 is the Line Grounding Strap. This two-position strap grounds P1-56 (a Main Interconnect board line) during normal operation.

DIRECT/INDIRECT INTERRUPT STRAP

W2098 is the Direct/Indirect Interrupt Strap. This two-position strap provides indirect addressing of interrupts during normal operation. If the run is cut between pins 1 and 2 and a strap placed between pins 2 and 3, direct addressing is selected.

BOOTSTRAP LIMITING STRAP

W2017 is the Bootstrap Limiting Strap. This two-position strap selects a 2K-byte address space within the Boot ROM during normal operation. If the run is cut between pins 1 and 2 and a strap is soldered between pins 2 and 3, only a 1K-byte address space within the Boot ROM is selected.

HIGH-SPEED INTERFACE STRAP

W1306 is the High-Speed Interface Strap. This single-position strap selects an 8-bit data character length during normal operation. If a strap is soldered across this position, a 7-bit data character length is selected.

STOP BIT SELECT STRAP

W1308 is the Stop Bit Select Strap. This single-position cuttable run selects one stop bit during normal operation. If the run at this position is cut, two stop bits are selected.

PARITY INHIBIT STRAP

W1309 is the Parity Inhibit Strap. This single-position cuttable run enables parity generation and checking during normal operation. If the run at this position is cut, the parity generation and checking functions are disabled.

EVEN/ODD PARITY STRAP

W1304 is the Even/Odd Parity Strap. This single-position strap selects even parity bits during normal operation. If a strap is soldered across this position and W1309 has not been cut, odd parity bits are selected.

DIAGNOSTIC MODE SWITCH

S1100 is the Diagnostic Mode Switch. This 6-position DIP switch is used to select the power-up mode of operation and the boot mode. For normal operation the six switch positions should be set as follows:

Switch S1100 Positions No.	Switch Setting	Switch Setting Selects
6	0	Normal Boot Mode
5	0	Run Power-up Diagnostics
4	0	Branch to CFM or display ROM-Based Diagnostic on error
3	1	8540 Boot
2	0	Not used set to "0"
1	0	Boot in Local Mode execute STARTUP string

NOTE

A switch setting of "0" is ON (or CLOSED). A switch setting of "1" is OFF (or OPEN).

DIAGNOSTIC LEDS

These LEDs are illuminated while the Power-Up Diagnostics are running. They indicate which test is in progress. If an error is detected, an error code is displayed on the LEDs. These LEDs are used in conjunction with the LEDs on the System RAM board.

EMULATOR CONTROLLER BOARD CONFIGURATION

Figure 7-2 shows the locations of jumpers and straps on the Emulator Controller board, and the type of connector at each location. There are five jumpers and five straps on the Emulator Controller board. Table 7-3 lists the jumper and strap configuration required for normal operation.

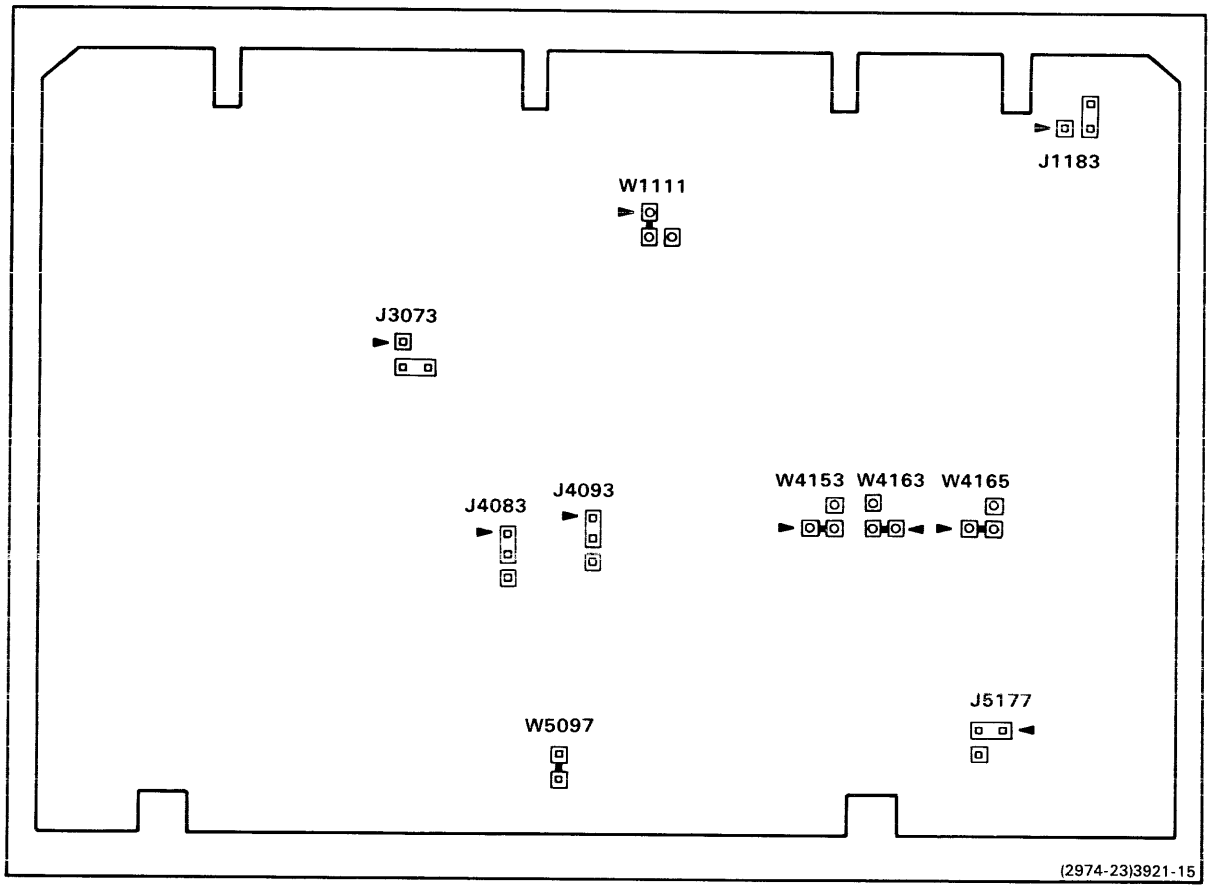

Fig. 7-2. Emulator Controller board jumpers and straps.

Table 7-3
Emulator Controller Board Normal Operating Configuration

Number	Jumper or Strap	Normal Operating Configuration
J1183	Front Panel Hold Jumper	Jumper across pins 2 and 3
J3073	Direct Interrupt Jumper	Jumper across pins 2 and 3
J4083	BP1 Extended Address Jumper	Jumper across pins 1 and 2
J4093	BP2 Extended Address Jumper	Jumper across pins 1 and 2
J5177	SVC Detection Jumper	Jumper across pins 1 and 2
W1111	Extended Address Strap	No change in original strapping
W4153	Immediate Interrupt Strap	No change in original strapping
W4163	Forced Jump Option Strap	No change in original strapping
W4165	Forced Jump Option Strap	No change in original strapping
W5097	Line Grounding Strap	No change in original strapping

FRONT PANEL HOLD JUMPER

J1183 is the Front Panel Hold Jumper. This two-position jumper enables or disables the front panel circuitry. Pins 1 and 2 enable the front panel circuitry. Pins 2 and 3 disable the front panel circuitry. For normal operation, place the jumper across pins 2 and 3.

EXTENDED ADDRESS STRAP

W1111 is the Extended Address Strap. This two-position strap enables the extended address function during normal operation. If the cuttable run between pins 1 and 2 is cut and a strap is soldered between pins 2 and 3, the extended address enable line is connected to a pull-up resistor and the extended address function is disabled.

LINE GROUNDING STRAP

W5097 is the Line Grounding Strap. This single-position cuttable run grounds P1-56 (a Main Interconnect board line) during normal operation.

BP1 EXTENDED ADDRESS JUMPER

J4083 is the BP1 Extended Address Jumper. This two-position jumper enables or disables the breakpoint 1 extended address function. Pins 1 and 2 enable the function. Pins 2 and 3 disable the function. For normal operation, place the jumper across pins 1 and 2.

BP2 EXTENDED ADDRESS JUMPER

J4093 is the BP2 Extended Address Jumper. This two-position jumper enables or disables the breakpoint 2 extended address function. Pins 1 and 2 enable the function. Pins 2 and 3 disable the function. For normal operation, place the jumper across pins 1 and 2.

SVC DETECTION JUMPER

J5177 is the SVC Detection Jumper. This two-position jumper selects SVC Detection support for all three emulation modes or for mode 0 only. Pins 1 and 2 select support for all modes. Pins 2 and 3 select support for mode 0 only. For normal operation, place the jumper across pins 1 and 2.

DIRECT/INDIRECT INTERRUPT JUMPER

J3073 is the Direct/Indirect Interrupt Jumper. This two-position jumper selects either direct or indirect addressing of interrupts. Pins 1 and 2 select direct addressing of interrupts. Pins 2 and 3 select indirect addressing of interrupts. For normal operation, place the jumper across pins 2 and 3.

IMMEDIATE INTERRUPT OPTION STRAP

W4153 is the Immediate Interrupt Option Strap. This two-position strap supports the current configuration of a single immediate interrupt and provides a method to incorporate an additional immediate interrupt if needed. If the cuttable run between pins 1 and 2 is cut and a strap is soldered between pins 2 and 3, INT 31 FF(H) is NORed with the current immediate interrupt at U4150.

FORCED JUMP OPTION STRAPS

W4163 and W4165 are the Forced Jump Option Straps. Future requirements to provide a forced jump capability to interrupts 30 and/or 31 can be met by cutting the run between pins 1 and 2 and soldering a strap between pins 2 and 3 of each strap.

SYSTEM RAM BOARD CONFIGURATION

Figure 7-3 shows the location of the two jumpers and eight LEDs on the System RAM board. Table 7-4 lists the jumper configuration required for normal operation.

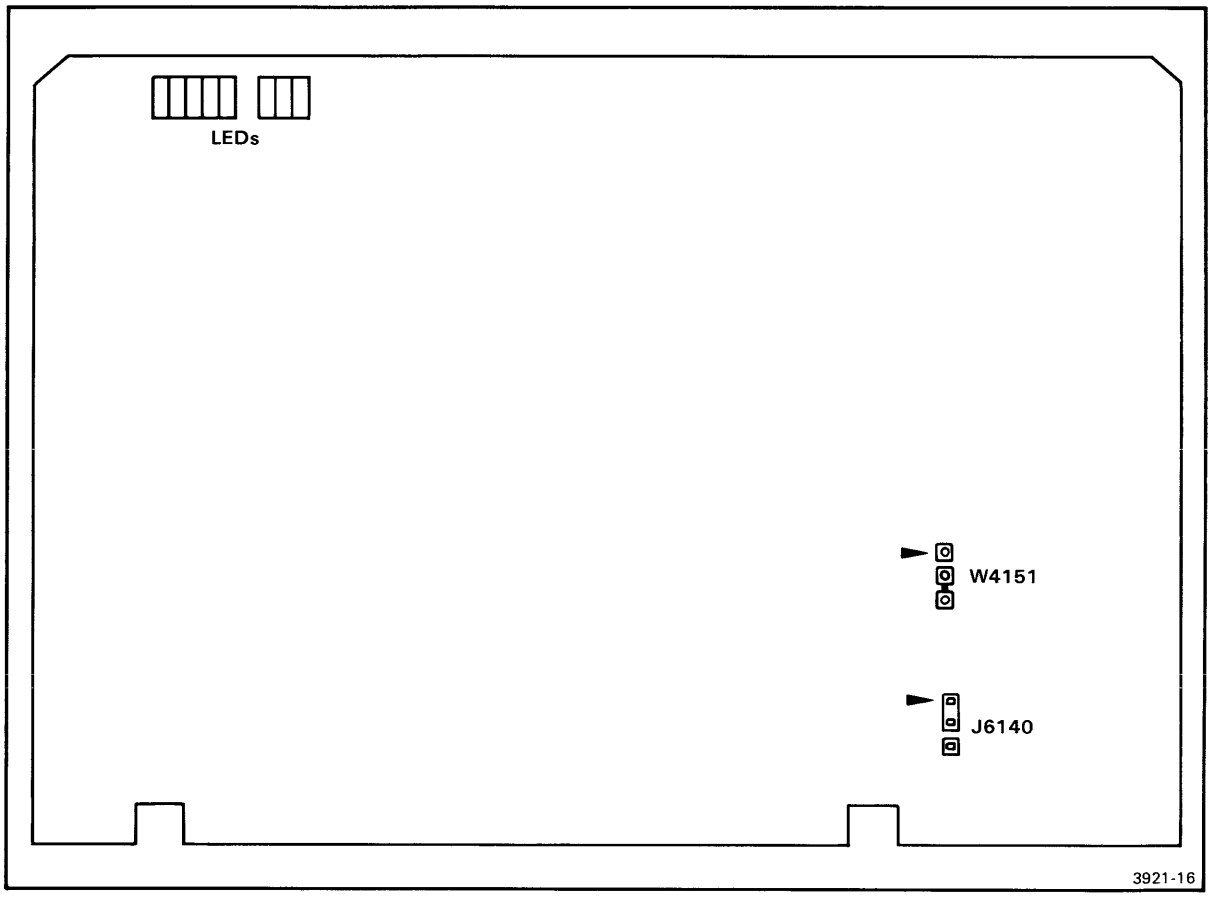

Fig. 7-3. System RAM board jumpers and straps.

Table 7-4
System RAM Board Normal Operating Configuration

Number	Jumper or Strap	Normal Operating Configuration
J6140	Test Jumper	Jumper across pins 1 and 2
W4151	Developmental Strap	No change in original strapping

TEST JUMPER

J6140 is the Test Jumper. This two-position jumper determines the board's response to the CMEM(H) line. Pins 1 and 2 select the board as System Memory whenever the CMEM(H) line goes low. For special applications, pins 2 and 3 select the board as Program Memory. In this configuration diagnostics that test various program memory functions can be conducted on the board when the CMEM(H) line goes high. When testing the board using diagnostics, the board is physically located in the System section of the Main Interconnect board. For normal operations, place the jumper across pins 1 and 2.

DEVELOPMENTAL STRAP

W4151 is a strap that may be used for special developmental requirements. This two-position strap permits MSTR RUN(L) and OPREQ(L) to control the timing of the board. If the cuttable run between pins 2 and 3 is cut and a strap is soldered between pins 1 and 2, MSTR RUN(L) is removed from the board.

DIAGNOSTIC LEDS

Five of these eight LEDs are turned off or on while the Power-Up Diagnostics are running. The five LEDs indicate which test is in progress; if an error is detected, an error code is displayed on the LEDs. These LEDs are used in conjunction with the LEDs on the System Controller board. The other three LEDs monitor the status of the lower three bits from the data byte of I/O port address D2.

SYSTEM ROM BOARD CONFIGURATION

Figure 7-4 shows the configuration of the System ROM board. It also shows the location of the test point TP Vpp, the 32 ROM sockets, and the test point connector, J1111. Test point TP Vpp is used to determine if the correct voltage and timing is applied to the EEPROMs during an erase or programming operation. Test point connector J1111 contains nine TTL test points. This harmonica-type connector provides easy termination of a logic analyzer or similar test equipment. Table 7-5 lists the nine TTL test points.

The System ROM board has no jumper positions. However, there are five two-position strap configurations located directly below 30 of the 32 ROM sockets. Refer to Fig. 7-4. The strap configurations are used to configure each ROM socket for a specified PROM type.

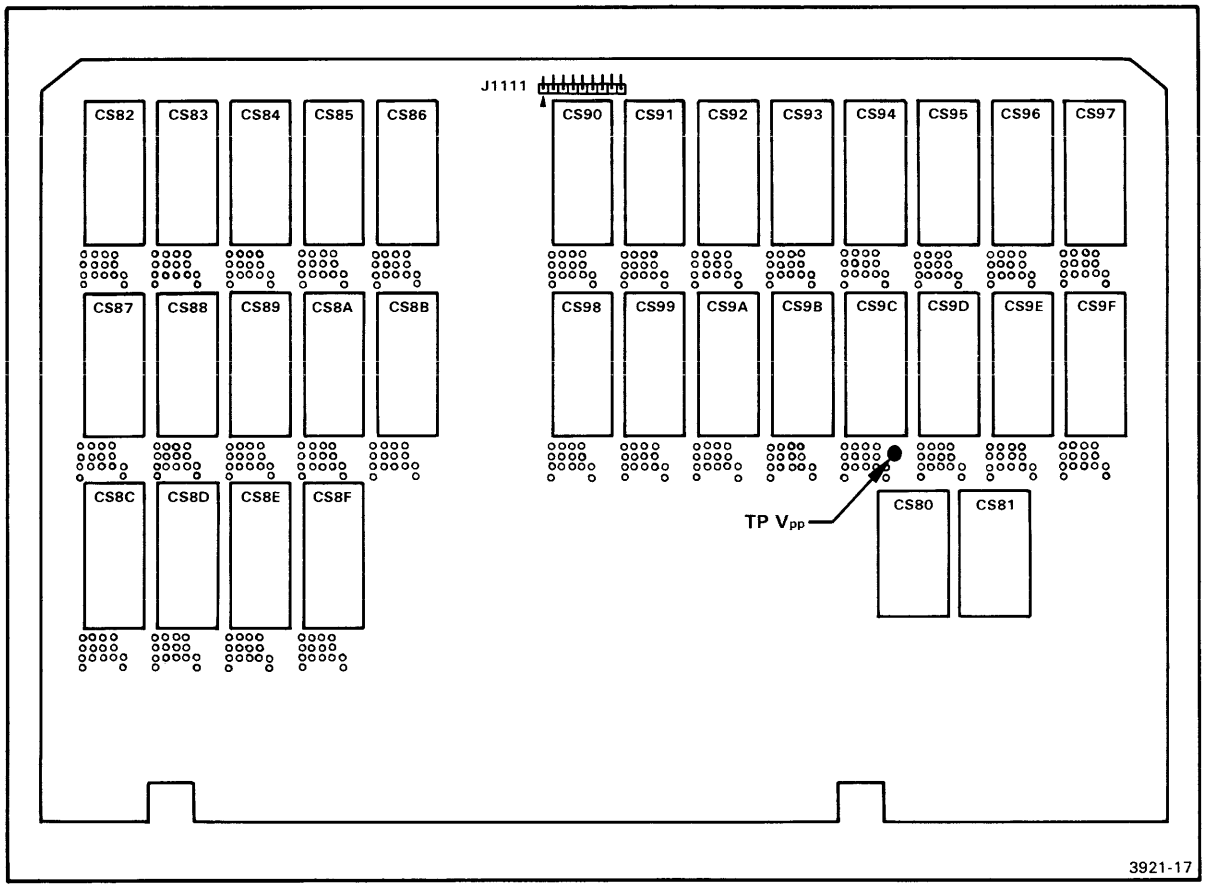

Fig. 7-4. System ROM board jumpers and straps.

Table 7-5
J1111 -- TTL Test Points

Pin No.	Designation	Function
1	GND	Logic ground.
2	STAT	Status--During a read to I/O port address D8, data bit D5 is high when the EEPROMs are being programmed or erased.
3	BD EN	Board Enable--When data bit D7 of I/O port address D8 is set high, the ROM array is enabled.
4	EE EN	EEPROM Enable--When data bit D6 of I/O port address D8 is set high, the EEPROM array is enabled.
5	Vpp	When high, EEPROMs are being programmed or erased.
6	BD BUF	Board Buffer--When low, buffer U4090 is enabled ,forcing the data byte onto the system data bus.
7	EE BUF	EEPROM Buffer--When low, address and data latches are enabled during a write operation (programming or erasing) to the EEPROMs.
8	WRP MD	Write Pulse Modified--Clocks the D-type flip-flop when going from low to high, at the start of a programming or erase cycle.
9	EE WR	EEPROM Write--When high at the same time WRP(H) is high, generates the WRP MD (Write Pulse Modified) pulse (pin no. J1111-8).

NOTE

The test point TP Vpp (shown in Fig. 7-4) and pin no. J1111-5 (also designated Vpp) are not the same test point. TP Vpp is the actual dc voltage applied to the EEPROM devices. Pin no. J1111-5 is a TTL test point. The timing relationships of the two test points, however, are identical.

ROM-SOCKET STRAPS

Figure 7-5 shows the two-position strap configurations for each of the three PROM types. Each ROM socket is configured for the type-2764 PROM when the board is manufactured. If a type-2732A or type-27128 PROM is used, W5 must be strapped accordingly. Table 7-6 lists the strap configuration required for normal operation.

NOTE

Designations W1 through W5 and arrow heads (to indicate pin 1) are added to Fig. 7-5 for clarity purposes. The arrow head and strap designations are not on the actual circuit board.

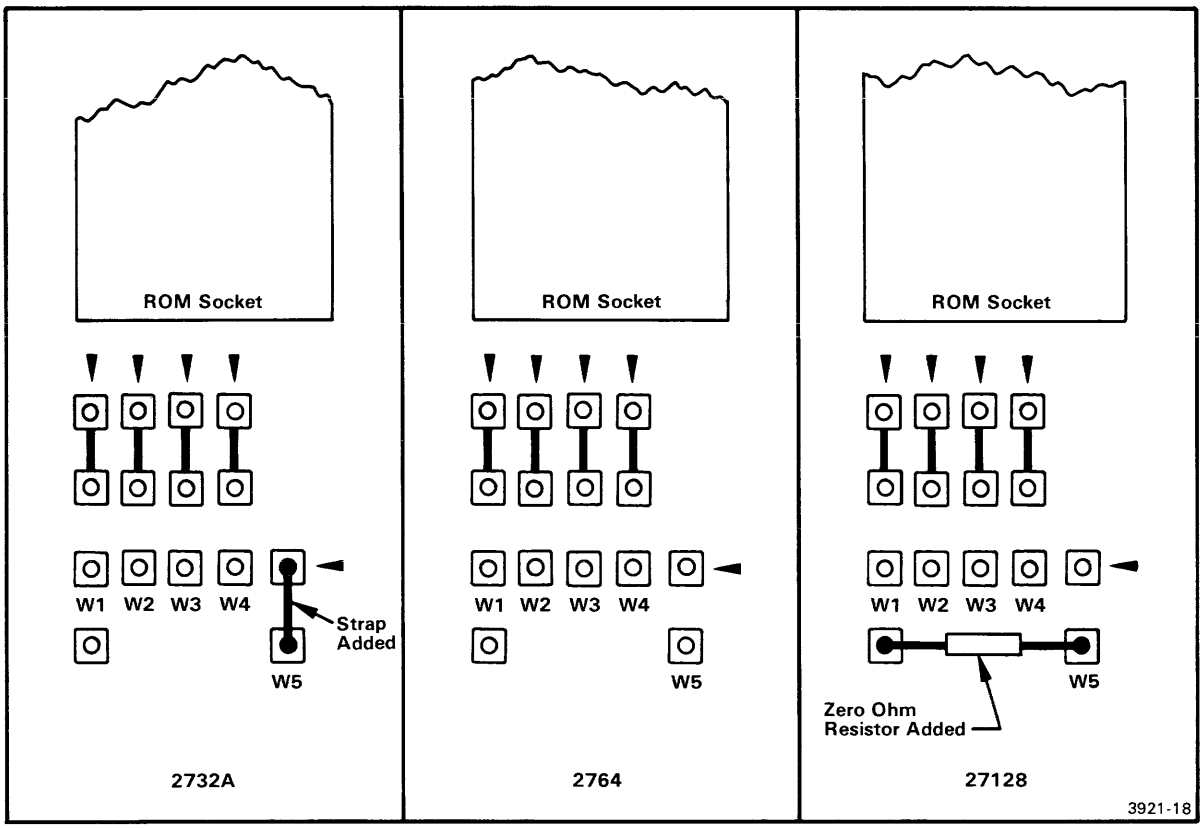

Fig. 7-5. Strapping configurations for specified PROM types.

Table 7-6
System ROM Board Normal Operating Configuration

Strap Number	PROM Types	Normal Operation Configuration
W1--W4	2732A 2764 27128	No change in original strapping
W5	2764	No change in original strapping
W5	2732A	Strap across pins 1 and 2
W5	27128	Zero-ohm resistor across pins 2 and 3.

INSTALLATION OF ROMS

When you receive your 8540, the EEPROMs and ROMs are installed in the System ROM board for the basic system and any optional boards ordered with your basic unit. Refer to Fig. 7-4. The EEPROMs are installed in sockets CS80 and CS81. The remainder of the sockets (CS82--CS9F) are for the operating system ROMs, diagnostic ROMs, and optional equipment ROMs.

There is no requirement for the ROMs to be installed in specific sockets; however, the operating system ROMs are normally in the lower numbered sockets: CS82 and up. The diagnostic ROMs are next, leaving the remaining sockets for options.

The 8540 is designed to accommodate two emulator boards. This means that any two 8-bit or 16-bit emulators (one board each) can be installed. However, only one 16-bit emulator consisting of more than one board can be installed at a time.

The spare ROM sockets for optional equipment are also limited. You may have to remove existing ROMs and install other ROMs when you add or replace the emulator board(s). This will depend on the options installed in your 8540.

CAUTION

Procedures for the removal or installation of devices are also applicable to the ROMs. The body of the ROM should remain parallel to the circuit board during removal or installation. Do not rock or tilt the ROM when removing or installing. Make sure pin 1 of the ROM is inserted in pin 1 of the socket.

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PROGRAM MEMORY BOARD CONFIGURATION

Figure 7-6 shows the locations of the jumpers, straps, and switch on the Program Memory board, and the type of connector at each location. There are four jumpers and two straps on the Program Memory board. In addition, a DIP switch (S7170) is used to select the extended addressing function. Table 7-7 lists the jumper and strap configuration required for normal operations.

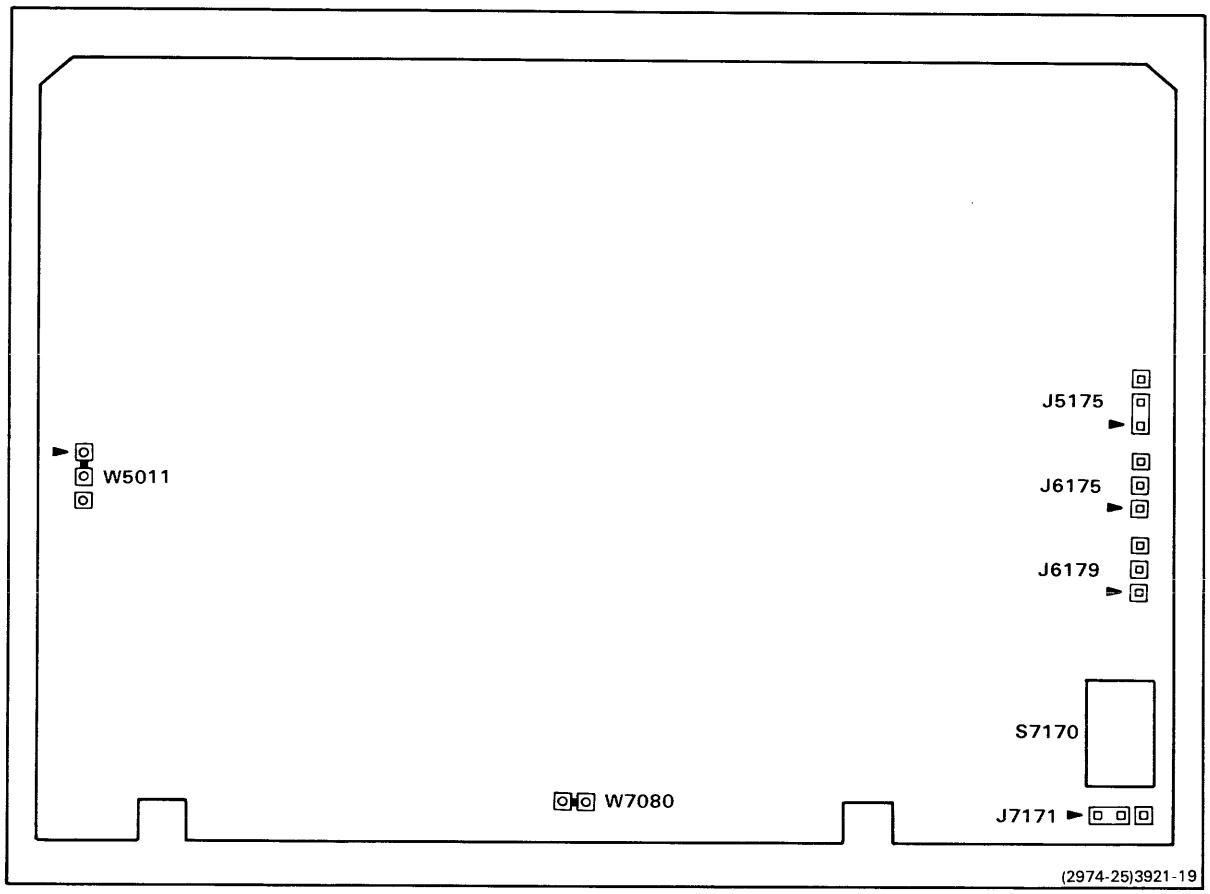

Fig. 7-6. Program Memory board jumpers and straps.

Table 7-7
Program Memory Board Normal Operating Configuration

Number	Jumper or Strap	Normal Operating Configuration
J5175	Memory Relocation Jumper	See text description
J6175	Low/High Board Jumper	See text description
J6179	Program/System Memory Jumper	Jumper across pins 1 and 2
J7171	Extended Bank Jumper	Jumper across pins 1 and 2
W5011	Delayed Read Strap	No change in original strapping
W7080	Line Grounding Strap	No change in original strapping
S7170	Extended Memory DIP Switch	See text description

PROGRAM/SYSTEM MEMORY JUMPER

J6197 is the Program/System Memory Jumper. This two-position jumper determines whether the board is used as Program Memory or, for special applications, as System Memory. Pins 1 and 2 select Program Memory. Pins 2 and 3 select a special System Memory configuration. The 8540 operating system, OS/40, prohibits using the Program Memory board as System Memory. Therefore, for normal operations, place the jumper across pins 1 and 2.

LOW/HIGH BOARD JUMPER

J6175 is the Low/High Board Jumper. This two-position jumper determines whether the board will be used as low memory (addresses 0 to 32K) or high memory (addresses 32K to 64K). Pins 1 and 2 select high memory. Pins 2 and 3 select low memory.

EXTENDED BANK JUMPER

J7171 is the Extended Bank Jumper. This two-position jumper enables or disables the extended bank comparator function. Pins 1 and 2 enable this function. Pins 2 and 3 disable the function. For normal operation, place the jumper across pins 1 and 2.

MEMORY RELOCATION JUMPER

J5175 is the Memory Relocation Jumper. This two-position jumper enables or disables the memory relocation function. Pins 1 and 2 enable the function. Pins 2 and 3 disable the function. For Program Memory normal operation with one memory board installed, place the jumper across pins 1 and 2. When two Program Memory boards are installed, place the jumpers on both boards across pins 2 and 3.

DELAYED READ STRAP

W5011 is the Delayed Read Strap. If the cuttable run between pins 1 and 2 is cut and a strap soldered between pins 2 and 3, the READ ENBL(L) signal will no longer be delayed. This signal is delayed during normal operation.

LINE GROUNDING STRAP

W7080 is the Line Grounding Strap. This single-position cuttable run grounds P1-56 (a Main Interconnect board line) during normal operation.

EXTENDED MEMORY DIP SWITCH

S7170 is the Extended Memory DIP switch. This 8-bit DIP switch works in conjunction with the Low/High Jumper to allocate extended memory. Unless a particular setting for an option is indicated within that option's Installation Manual, all switches should be in the ON or CLOSED position.

COMMUNICATIONS INTERFACE BOARD CONFIGURATION

Figure 7-7 shows the locations of jumpers on the Communications Interface board and the type of connector at each location. There are three jumpers on the Communications Interface board. Table 7-8 lists the configuration required for normal operation.

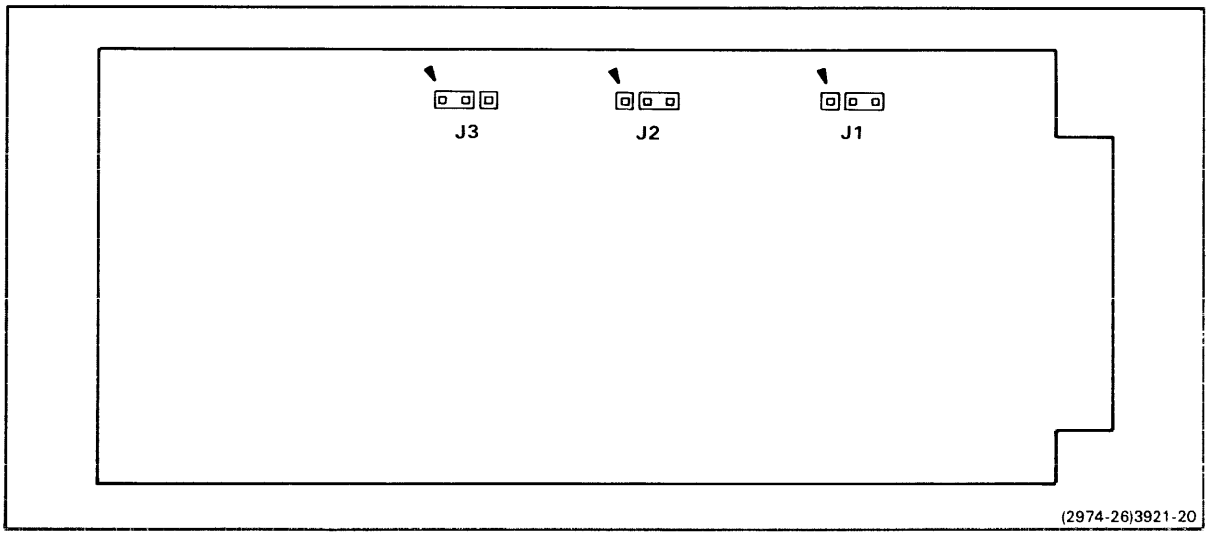

Fig. 7-7. Communications Interface board jumpers.

Table 7-8
Communications Interface Board Normal Operating Configuration

Number	Jumper or Strap	Normal Operating Configuration
J1	RS-232-C Multiplexer Jumper	Jumper across pins 2 and 3
J2	RS-232-C Multiplexer Jumper	Jumper across pins 2 and 3
J3	External Baud Rate Jumper	Jumper across pins 1 and 2

RS-232-C CONTROL LINE MULTIPLEXER JUMPER (J102)

J1 (located on the Communications Interface board) is the RS-232-C Control Line Multiplexer Jumper for jack J102 (located on the rear panel). This two-position jumper selects the RTS(H) signal or ground as a control signal for J102. Pins 1 and 2 select the RTS(H) signal. Pins 2 and 3 select ground. For normal operation, place the jumper across pins 2 and 3.

RS-232-C CONTROL LINE MULTIPLEXER JUMPER (J101)

J2 (located on the Communications Interface board) is the RS-232 Control Line Multiplexer Jumper for jack J101 (located on the rear panel). This two-position jumper selects the CTS(H) signal or ground as a control signal for J101. Pins 1 and 2 select the CTS(H) signal. Pins 2 and 3 select ground. For normal operation, place the jumper across pins 2 and 3.

EXTERNAL BAUD CLOCK JUMPER

J3 (located on the Communications Interface board) is the External Baud Clock Jumper. This two-position jumper selects either 110 baud rate or an external baud rate clock. Pins 1 and 2 select a signal from the 110 baud rate generator. Pins 2 and 3 disconnect the line from the 110 baud rate generator and select an external signal as the baud rate. For normal operation, place the jumper across pins 1 and 2.